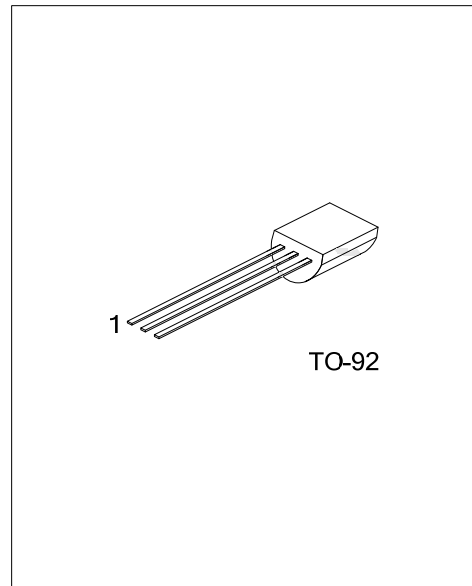




## MCR101

SCR

### SENSITIVE GATE SILICON CONTROLLED RECTIFIERS REVERSE BLOCKING THYRISTORS



#### DESCRIPTION

PNPN devices designed for high volume, line-powered consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thrusters, and sensing and detection circuits. Supplied in an inexpensive plastic TO-92 package which is readily adaptable for use in automatic insertion equipment.

#### FEATURES

- \*Sensitive Gate Allows Triggering by Micro Controllers and other Logic Circuits
- \*Blocking Voltage to 600V
- \*On-State Current Rating of 0.8A RMS at 80°C
- \*High Surge Current Capability – 10A
- \*Minimum and Maximum Values of IGT, VGT and IH Specified for Ease of Design
- \*Immunity to dV/dt – 20V/μsec Minimum at 110°C
- \*Glass-Passivated Surface for Reliability and Uniformity

#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
MCR101L-4-T92-B	MCR101G-4-T92-B	TO-92	G	A	K	Tape Box
MCR101L-4-T92-K	MCR101G-4-T92-K	TO-92	G	A	K	Bulk
MCR101L-6-T92-B	MCR101G-6-T92-B	TO-92	G	A	K	Tape Box
MCR101L-6-T92-K	MCR101G-6-T92-K	TO-92	G	A	K	Bulk
MCR101L-8-T92-B	MCR101G-8-T92-B	TO-92	G	A	K	Tape Box
MCR101L-8-T92-K	MCR101G-8-T92-K	TO-92	G	A	K	Bulk

Note: Pin Assignment: G: Gate A: Anode K: Cathode

<p>MCR101G-4-T92-B</p>	<p>(1) B: Tape Box, K: Bulk  (2) T92: TO-92  (3) 4: 200V, 6: 400V, 8: 600V  (4) G: Halogen Free and Lead Free, L: Lead Free</p>
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■ MARKING

MCR101-4	MCR101-6	MCR101-8
<p>The diagram shows a rectangular marking area for the MCR101-4 component. It contains the text 'UTC' at the top, 'MCR101' followed by a small square symbol, and '-4' followed by three small square symbols. Below this is the number '1'. To the right of the marking area, three arrows point to the text: 'L: Lead Free', 'G: Halogen Free', and 'Date Code'.</p>	<p>The diagram shows a rectangular marking area for the MCR101-6 component. It contains the text 'UTC' at the top, 'MCR101' followed by a small square symbol, and '-6' followed by three small square symbols. Below this is the number '1'. To the right of the marking area, three arrows point to the text: 'L: Lead Free', 'G: Halogen Free', and 'Date Code'.</p>	<p>The diagram shows a rectangular marking area for the MCR101-8 component. It contains the text 'UTC' at the top, 'MCR101' followed by a small square symbol, and '-8' followed by three small square symbols. Below this is the number '1'. To the right of the marking area, three arrows point to the text: 'L: Lead Free', 'G: Halogen Free', and 'Date Code'.</p>

### ■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Peak Repetitive Off-State Voltage(note) ( $T_J = -40$ to $110^\circ\text{C}$ , Sine Wave, 50 to 60Hz; Gate Open)	MCR101-4	200	V
	MCR101-6	400	
	MCR101-8	600	
On-State RMS Current ( $T_C = 80^\circ\text{C}$ ) 180° Condition Angles	$I_{T(RMS)}$	0.8	A
Peak Non-Repetitive Surge Current (1/2 cycle, Sine Wave, 60Hz, $T_J = 25^\circ\text{C}$ )	$I_{TSM}$	10	A
Circuit Fusing Considerations ( $t = 8.3$ ms)	$I^2t$	0.415	$\text{A}^2\text{s}$
Forward Peak Gate Power ( $T_A = 25^\circ\text{C}$ , Pulse Width $\leq 1.0\mu\text{s}$ )	$P_{GM}$	0.1	W
Forward Average Gate Power ( $T_A = 25^\circ\text{C}$ , $t = 8.3\text{ms}$ )	$P_{G(AV)}$	0.1	W
Peak Gate Current – Forward ( $T_A = 25^\circ\text{C}$ , Pulse Width $\leq 1.0\mu\text{s}$ )	$I_{GM}$	1	A
Peak Gate Voltage – Reverse ( $T_A = 25^\circ\text{C}$ , Pulse Width $\leq 1.0\mu\text{s}$ )	$V_{GRM}$	5	V
Operating Junction Temperature @ Rated $V_{RRM}$ and $V_{DRM}$	$T_J$	-40 ~ +110	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-40 ~ +150	$^\circ\text{C}$

Note:  $V_{DRM}$  and  $V_{RRM}$  for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

### ■ THERMAL DATA

PARAMETER	SYMBOL	RATING	UNIT
Junction to Ambient	$\theta_{JA}$	200	$^\circ\text{C/W}$
Junction to Case	$\theta_{JC}$	75	$^\circ\text{C/W}$

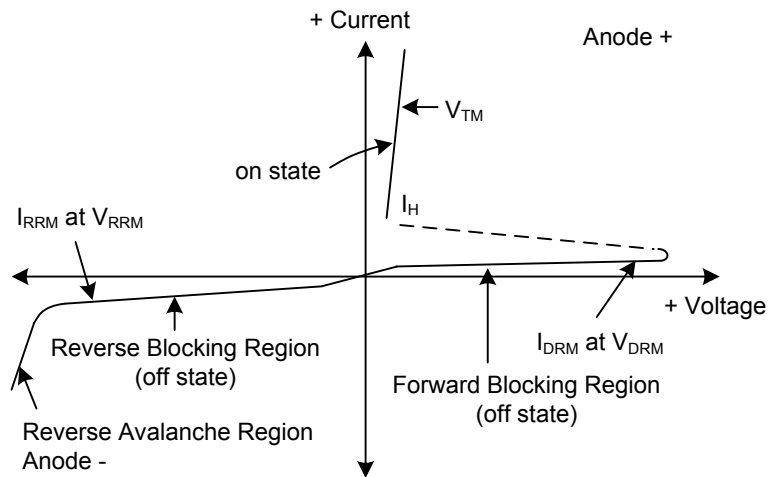
### ■ ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise stated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF CHARACTERISTICS</b>						
Peak Forward or Reverse Blocking Current	$I_{DRM}, I_{RRM}$	$V_D = \text{Rated } V_{DRM} \text{ and } V_{RRM}; R_{GK} = 1\text{k}\Omega$			10	$\mu\text{A}$
					100	
<b>ON CHARACTERISTICS</b>						
Peak Forward On-State Voltage (Note1)	$V_{TM}$	$I_{TM} = 1\text{A Peak @ } T_A = 25^\circ\text{C}$			1.7	V
Gate Trigger Current (Continuous dc)	$I_{GT}$	$V_{AK} = 7\text{Vdc}, R_L = 100\Omega, T_C = 25^\circ\text{C}$	30		100	$\mu\text{A}$
Holding Current	$I_H$	$V_{AK} = 7\text{Vdc}, \text{initiating current} = 20\text{mA}$		0.5	5	mA
					10	
Latch Current	$I_L$	$V_{AK} = 7\text{V}, I_g = 200\mu\text{A}$		0.6	10	mA
					15	
Gate Trigger Current (continuous dc)	$V_{GT}$	$V_{AK} = 7\text{Vdc}, R_L = 100\Omega$		0.62	0.8	V
					1.2	
<b>DYNAMIC CHARACTERISTICS</b>						
Critical Rate of Rise of Off-State Voltage	$dV/dt$	$V_D = \text{Rated } V_{DRM}, \text{Exponential Waveform}, R_{GK} = 1000\Omega, T_J = 110^\circ\text{C}$	20	35		$\text{V}/\mu\text{s}$
Critical Rate of Rise of On-State Current	$di/dt$	$I_{PK} = 20\text{A}, P_w = 10\mu\text{sec}, diG/dt = 1\text{A}/\mu\text{sec}, I_{gt} = 20\text{mA}$			50	$\text{A}/\mu\text{s}$

Note: Indicates Pulse Test Width  $\leq 1.0\text{ms}$ , duty cycle  $\leq 1\%$

■ VOLTAGE CURRENT CHARACTERISTIC OF SCR

SYMBOL	PARAMETER
$V_{DRM}$	Peak Repetitive Off Stat Forward Voltage
$I_{DRM}$	Peak Forward Blocking Current
$V_{RRM}$	Peak Repetitive Off State Reverse Voltage
$I_{RRM}$	Peak Reverse Blocking Current
$V_{TM}$	Peak On State Voltage
$I_H$	Holding Current



## TYPICAL CHARACTERISTICS

Figure 1. Typical Gate Trigger Current versus Junction Temperature

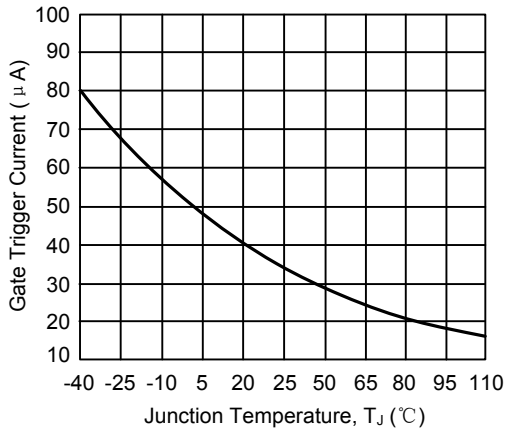


Figure 2. Typical Gate Trigger Voltage versus Junction Temperature

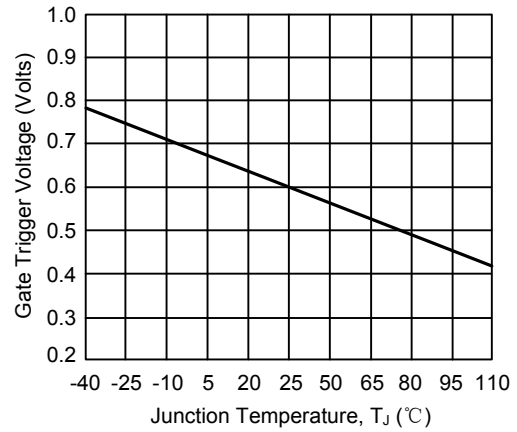


Figure 3. Typical Holding Current versus Junction Temperature

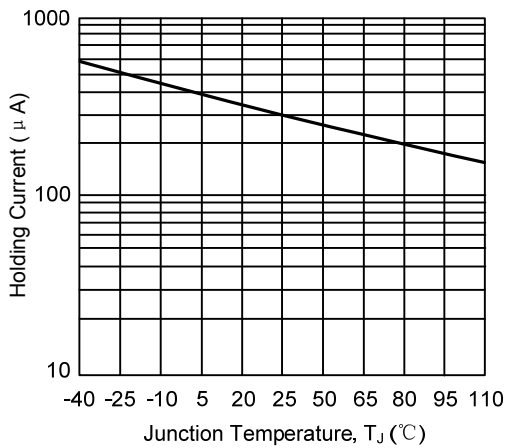


Figure 4. Typical Latching Current versus Junction Temperature

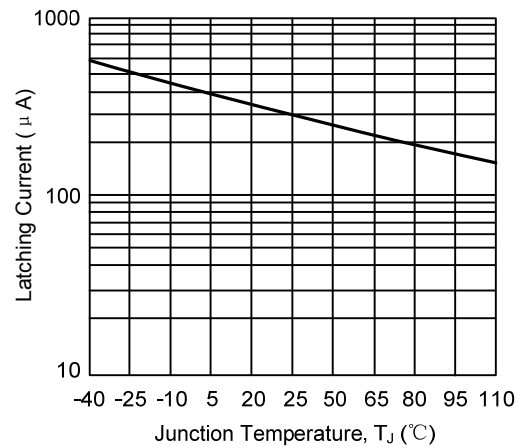


Figure 5. Typical RMS Current Derating

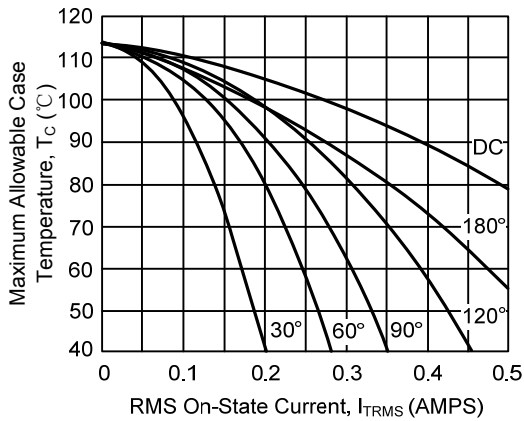
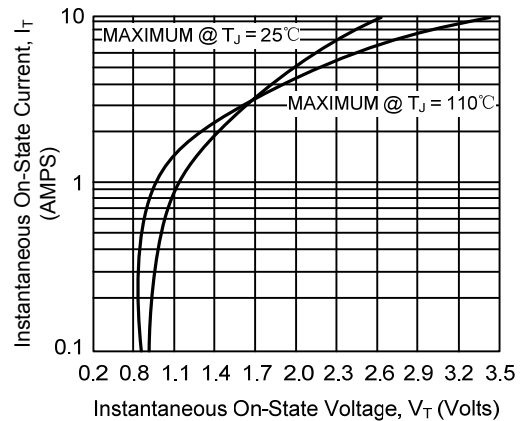


Figure 6. Typical On-State Characteristics



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