

U74HCT640

CMOS IC

OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

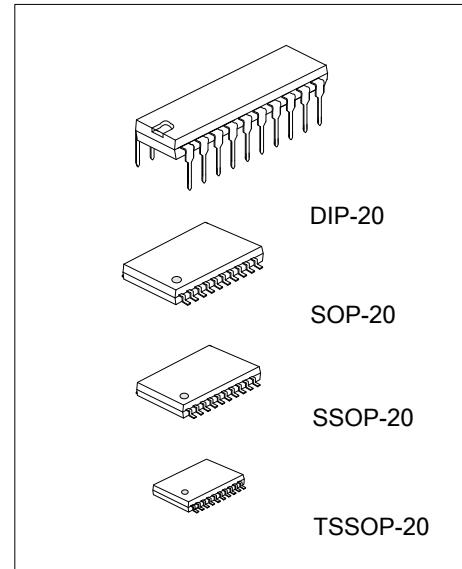
■ DESCRIPTION

The **U74HCT640** is a octal bus transceivers with 3-state outputs. It is designed for asynchronous two-way communication between data buses. Depending on the direction-control (DIR) input, data are transmitted from the A bus to the B bus or from B bus to the A bus.

When \overline{OE} is high, the buses are effectively isolated. When \overline{OE} is low, the buses are enable.

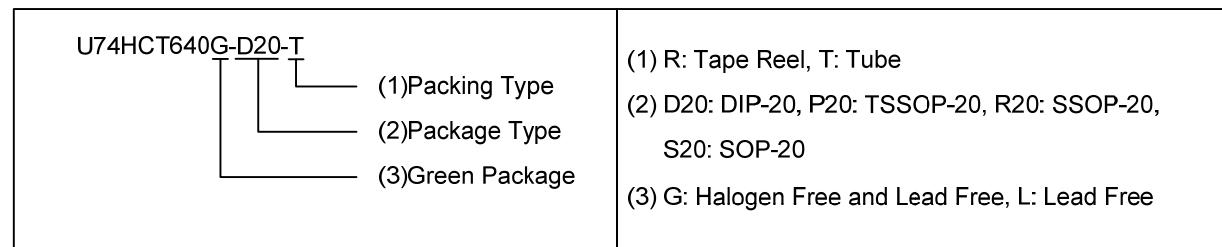
■ FEATURES

- * Inputs are TTL-voltage compatible
- * Typical t_{PD} of 12ns at 5.5V, $C_L=50pF$
- * Low power consumption, $I_{CC} = 8\mu A$ (Max) at 5.5V
- * $\pm 6mA$ output driver at 4.5V



■ ORDERING INFORMATION

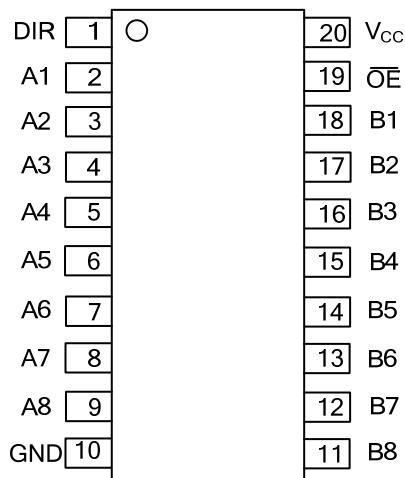
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HCT640L-D20-T	U74HCT640G-D20-T	DIP-20	Tube
U74HCT640L-S20-R	U74HCT640G-S20-R	SOP-20	Tape Reel
U74HCT640L-R20-R	U74HCT640G-R20-R	SSOP-20	Tape Reel
U74HCT640L-P20-R	U74HCT640G-P20-R	TSSOP-20	Tape Reel



■ MARKING

DIP-20	SOP-20 / SSOP-20 / TSSOP-20
<p>Detailed description: This diagram shows the marking on a DIP-20 package. It features a 20-pin grid with pins numbered 20 down to 11 from top-left to bottom-right. Above the grid, the code 'U74HCT640' is printed, with 'UTC' above it and 'D20' below it. Below the grid, there are two small squares, one above the other. Arrows point to specific markings: 'Date Code' points to the 'UTC' and square pairs; 'L: Lead Free' points to the 'D' in 'D20'; 'G: Halogen Free' points to the second square; and 'Lot Code' points to the numbers 1 through 10 at the bottom of the grid.</p>	<p>Detailed description: This diagram shows the marking on a SOP-20, SSOP-20, or TSSOP-20 package. It features a 20-pin grid with pins numbered 20 down to 11. Above the grid, the code 'U74HCT640' is printed, with 'UTC' above it and a small circle below it. Below the grid, there are two small squares, one above the other. Arrows point to specific markings: 'Date Code' points to the 'UTC' and square pairs; 'L: Lead Free' points to the small circle; 'G: Halogen Free' points to the second square; and 'Lot Code' points to the numbers 1 through 10 at the bottom of the grid.</p>

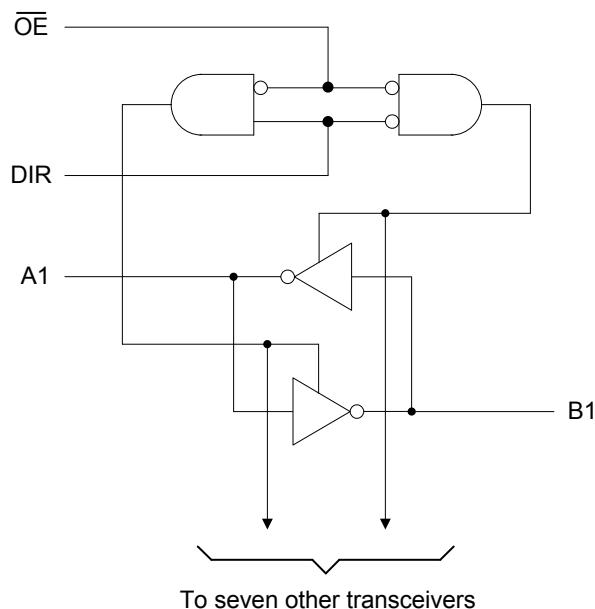
■ PIN CONFIGURATION



■ FUNCTION TABLE (each buffer)

INPUTS		OPERATION
OE	DIR	
L	L	\overline{B} data to A bus
L	H	A data to B bus
H	X	Isolation

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
Input Clamp Current ($V_{IN}<0$)	I_{IK}	± 20	mA
Output Clamp Current ($V_{OUT}<0$, or $V_{OUT}>V_{CC}$)	I_{OK}	± 20	mA
Output Current	I_{OUT}	± 25	mA
V_{CC} or GND Current	I_{CC}	± 50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5	5	5.5	V
High-Level Input Voltage	V_{IH}	$V_{CC} = 4.5V$ to 5.5V	2			V
Low-Level Input Voltage	V_{IL}	$V_{CC} = 4.5V$ to 5.5V	0		0.8	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise and Fall Times	t_R, t_F	$V_{CC} = 4.5V$	0		500	ns
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	$I_{OH}=-20\mu A, V_{CC}=4.5V$	4.4	4.499		V
		$I_{OH}=-6mA, V_{CC}=4.5V$	3.98	4.30		
Low-Level Output Voltage	V_{OL}	$I_{OL}=20\mu A, V_{CC}=4.5V$		0.001	0.1	V
		$I_{OL}=6mA, V_{CC}=4.5V$		0.17	0.26	
Input Leakage Current (DIR or \overline{OE})	$I_{I(LEAK)}$	$V_{IN}=V_{CC}$ or 0, $V_{CC}=5.5V$		± 0.1	± 100	μA
High-Impedance State Current (A or B)	I_{OZ}	$V_{OUT}=V_{CC}$ or 0, $V_{CC}=5.5V$		± 0.01	± 0.5	μA
Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or 0, $I_{OUT}=0$, $V_{CC}=5.5V$			8	μA
Additional Quiescent Supply Current	ΔI_{CC}	One input at 0.5V or 2.4V, other inputs at 0V or V_{CC} , $V_{CC}=5.5V$		1.4	2.4	mA
Input Capacitance (DIR or \overline{OE})	C_{IN}	$V_{IN}=V_{CC}$ or 0, $V_{CC}=4.5V$ to 5.5V		3	10	pF

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from A to B or B to A	t_{PD}	$V_{CC}=4.5V, C_L=50pF, R_L=1k\Omega$		14	21	ns
		$V_{CC}=5.5V, C_L=50pF, R_L=1k\Omega$		12	18	
Enable times from \overline{OE} to A or B	t_{EN}	$V_{CC}=4.5V, C_L=50pF, R_L=1k\Omega$		27	35	ns
		$V_{CC}=5.5V, C_L=50pF, R_L=1k\Omega$		24	32	
Disable times from \overline{OE} to A or B	t_{DIS}	$V_{CC}=4.5V, C_L=50pF, R_L=1k\Omega$		20	30	ns
		$V_{CC}=5.5V, C_L=50pF, R_L=1k\Omega$		18	26	
Output rise or fall time	t_T	$V_{CC}=4.5V, C_L=50pF, R_L=1k\Omega$		9	12	ns
		$V_{CC}=5.5V, C_L=50pF, R_L=1k\Omega$		8	11	

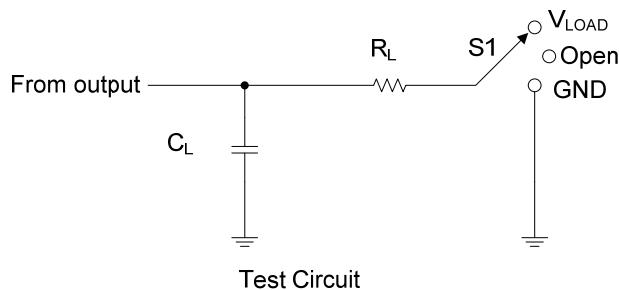
■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from A to B or B to A	t_{PD}	$V_{CC}=4.5V, C_L=150pF, R_L=1k\Omega$		17	27	ns
		$V_{CC}=5.5V, C_L=150pF, R_L=1k\Omega$		15	24	
Enable times from \overline{OE} to A or B	t_{EN}	$V_{CC}=4.5V, C_L=150pF, R_L=1k\Omega$		31	45	ns
		$V_{CC}=5.5V, C_L=150pF, R_L=1k\Omega$		28	41	
Output rise or fall time	t_T	$V_{CC}=4.5V, C_L=150pF, R_L=1k\Omega$		17	42	ns
		$V_{CC}=5.5V, C_L=150pF, R_L=1k\Omega$		14	38	

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

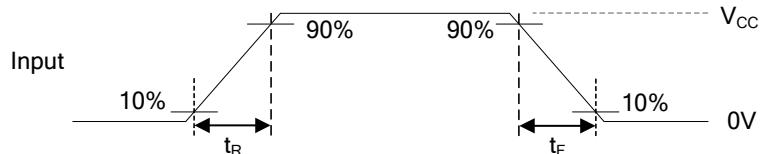
PARAMETER	SYMBOL	TEST CONDITIONS	TYP	UNIT
Power dissipation capacitance	C_{PD}	No load	40	pF

■ TEST CIRCUIT AND WAVEFORMS



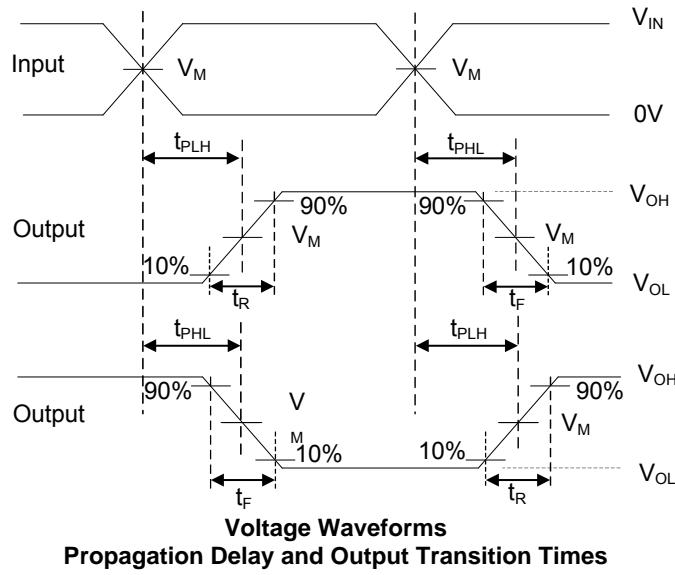
TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	Input		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
$5V \pm 0.5V$	V_{CC}	$\leq 6\text{ns}$	$V_{CC}/2$	V_{CC}	50pF 150pF	$1\text{k}\Omega$	$0.5V$

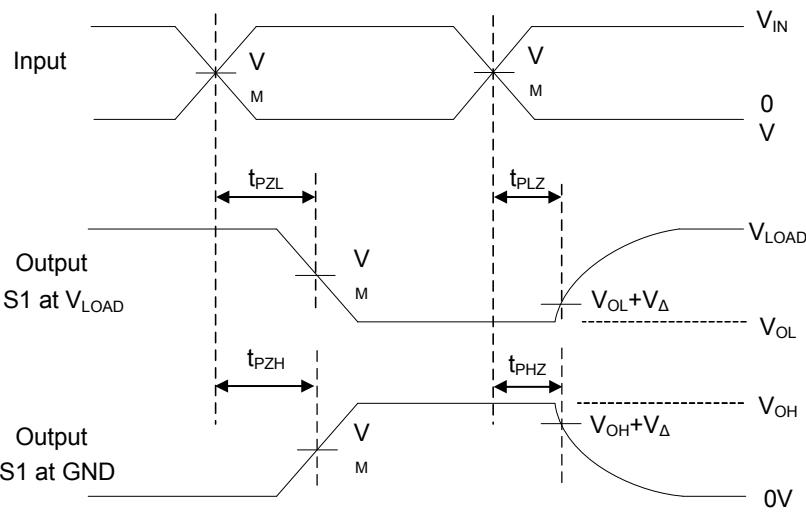


Voltage Waveforms Input Rise and Fall Times

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



**Voltage Waveforms
Propagation Delay and Output Transition Times**



Voltage Waveforms Enable and Disable Times

Notes:

1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_R=6\text{ns}$, $t_F=6\text{ns}$.
3. t_{PLH} and t_{PHL} are the same as t_{PD} .
4. t_{PLZ} and t_{PHZ} are the same as t_{DIS} .
5. t_{PZH} and t_{PLZ} are the same as t_{EN} .

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