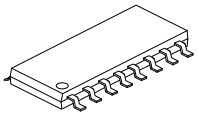
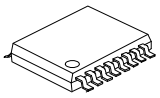
U74LVX4053

CMOS IC

TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXE



SOP-16



TSSOP-16

■ DESCRIPTION

The **U74LVX4053** is a high speed, low-voltage drive analog multiplexer/demultiplexer using silicon gate CMOS technology. In 3V and 5V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The **U74LVX4053** offer analog/digital signal selection as well as mixed signals wish a 4-Channel×2 configuration.

The switchses for each channel are turned on by the control pin digital signals.

Although the control signal logical amplitude (V_{CC}-GND) is small, the device can perform large-amplitude (V_{CC}-V_{EE}) signal switching.

For example, if V_{CC}=3V, GND=0V and V_{EE}=-3V, signals between -3V and +3V can be switched from the logical circuit using a signal 3V power supply.

All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forword side from the input to the V_{CC}). As a result, for example, 5V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the **U74LVX4053** can be used in a variety of applications, including in the system which has two power supplies, and in battery bachup circuits.

■ FEATURES

* Low ON resistance: R_{ON}=22Ω(Typ.)(V_{CC}-V_{EE}=3V)
* R_{ON}=15Ω(Typ.)(V_{CC}-V_{EE}=6V)
* High Speed: t_{pd}=3ns (Typ.)(V_{CC}=3V)
* Low power Dissipation: I_{CC}=4μA (Max.)(T_A=25°C)
* Input level: V_{IL}=0.8V(Max.)(V_{CC}=3V)
  V_{IH}=2.0V(Min.)(V_{CC}=3V)
* Power down protection is provided on all control inputs
* Pin and function compatible with U74HC4053

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVX4053L-S16-R	U74LVX4053G-S16-R	SOP-16	Tape Reel
U74LVX4053L-P16-R	U74LVX4053G-P16-R	TSSOP-16	Tape Reel

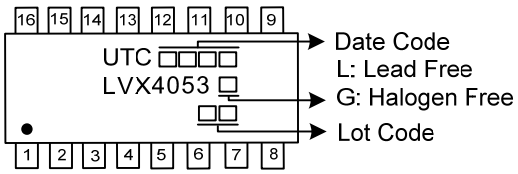
U74LVX4053G-S16-R

(1)Packing Type — (1) R: Tape Reel

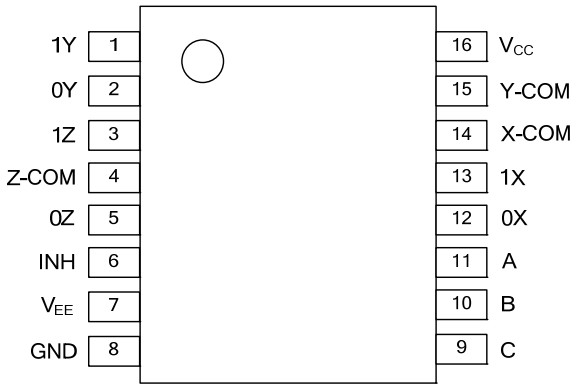
(2)Package Type — (2) S16: SOP-16, P16: TSSOP-16

(3)Green Package — (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ PIN CONFIGURATION

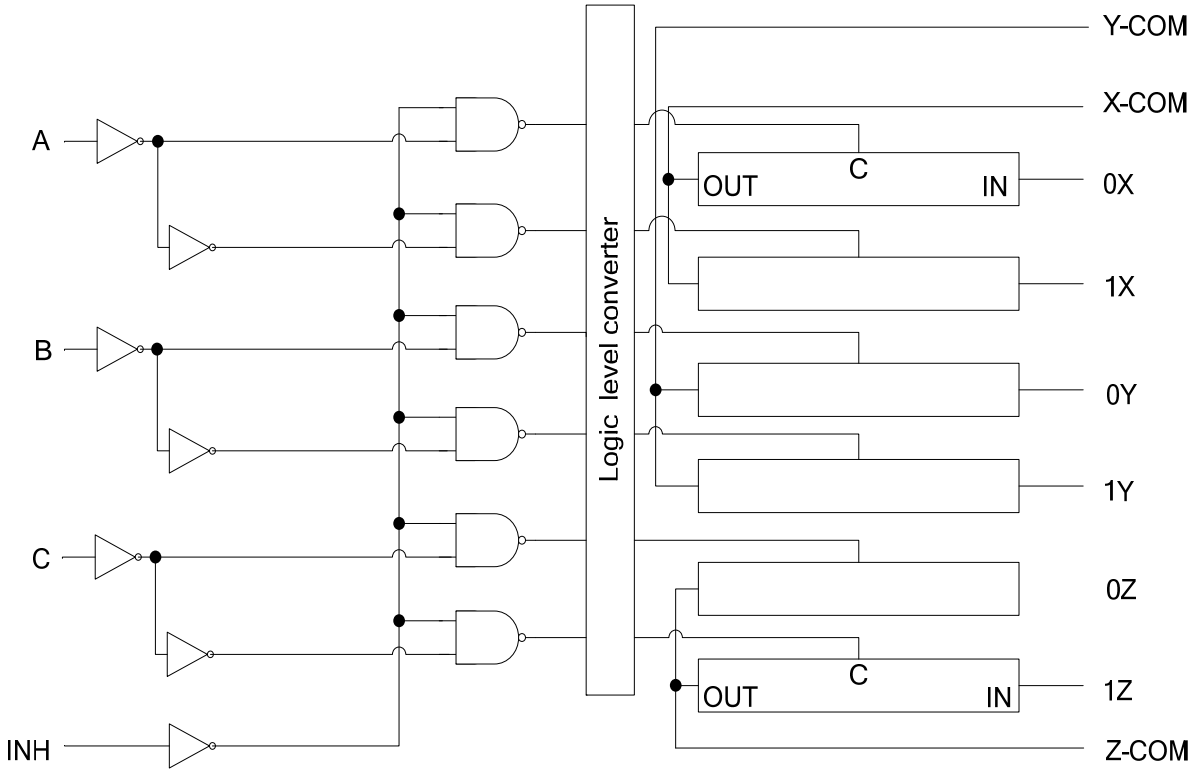


■ FUNCTION TABLE

CONTROL INPUTS				"ON" Channel
INH	C	B	A	LVX4053
L	L	L	L	0X,0Y,0Z
L	L	L	H	1X,0Y,0Z
L	L	H	L	0X,1Y,0Z
L	L	H	H	1X,1Y,0Z
L	H	L	L	0X,0Y,1Z
L	H	L	H	1X,0Y,1Z
L	H	H	L	0X,1Y,1Z
L	H	H	H	1X,1Y,1Z
H	X	X	X	None

Note: H: HIGH voltage level; L: LOW voltage level; X: Don't care

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Power Supply Voltage		V_{CC}	-0.5 ~ +7.0	V
		V_{CC}~V_{EE}	-0.5 ~ +7.0	V
Control Input Voltage		V_{IN}	-0.5 ~ +7.0	V
Switch I/O voltage		$V_{I/O}$	V_{EE}-0.5 ~ V_{CC}+0.5	V
Input diode current		I_{IK}	-20	mA
I/O diode Current		I_{IOK}	±20	mA
Switch through current		I_T	±25	mA
DC Vcc or ground current		I_{CC}	±50	mA
Power dissipation	SOP-16	P_D	500	mW
	TSSOP-16		450	mW
Storage Temperature		T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Voltage	V_{CC}		2.0		6.0	V
	V_{EE}		-4.0		0	V
	V_{CC}~V_{EE}		2.0		6.0	V
Input Voltage	V_{IN}		0		6.0	V
Switch I/O Voltage	$V_{I/O}$		V_{EE}		V_{CC}	V
Input Rise and Fall time	dt/dv	V_{CC}=3.3V±0.3	0		100	ns/V
		V_{CC}=5V±0.5	0		20	ns/V
Operating Temperature	T_A		-40		+125	°C

■ DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input voltage	High-level	V_{IH}	V_{CC}=2V		1.5			V
			V_{CC}=3V		2.0			V
			V_{CC}=4.5V		3.15			V
			V_{CC}=6V		4.2			V
	Low-level	V_{IL}	V_{CC}=2V				0.5	V
			V_{CC}=3V				0.8	V
			V_{CC}=4.5V				1.35	V
			V_{CC}=6V				1.8	V
ON resistance		R_{ON}	V_{IN}=V_{IL} or V_{IH} $V_{I/O}$=V_{CC} to V_{EE} $I_{I/O}$=2mA	V_{CC}=2V, V_{EE}=GND		200		Ω
				V_{CC}=3V, V_{EE}=GND		45	86	Ω
				V_{CC}=4.5V, V_{EE}=GND		24	37	Ω
				V_{CC}=3V, V_{EE}= -3V		17	26	Ω
			V_{IN}=V_{IL} or V_{IH} $V_{I/O}$=V_{CC} or V_{EE} $I_{I/O}$=2mA	V_{CC}=2V, V_{EE}=GND		28	73	Ω
				V_{CC}=3V, V_{EE}=GND		22	38	Ω
				V_{CC}=4.5V, V_{EE}=GND		17	27	Ω
				V_{CC}=3V, V_{EE}= -3V		15	24	Ω
Difference of ON resistance between switches		ΔR_{ON}	V_{IN}=V_{IL} or V_{IH} $V_{I/O}$=V_{CC} to V_{EE} $I_{I/O}$=2mA	V_{CC}=2V, V_{EE}=GND		10	25	Ω
				V_{CC}=3V, V_{EE}=GND		5	15	Ω
				V_{CC}=4.5V, V_{EE}=GND		5	13	Ω
				V_{CC}=3V, V_{EE}= -3V		5	10	Ω
Input/Output Leakage Current(switch off)		I_{OFF}	V_{OS}=V_{CC} or GND, V_{IS} =GND or V_{CC}, V_{IN}=V_{IH} OR V_{IL}	V_{CC}=3V, V_{EE}= GND			±0.25	μA
				V_{CC}=3V, V_{EE}= -3V			±0.5	μA
Quiescent Supply Current		I_{CC}	V_{IN}= V_{CC} or GND	V_{CC}=3V, V_{EE}= GND			4.0	μA
				V_{CC}=3V, V_{EE}= -3V			8.0	μA
Input/Output leakage current(switch on,output open)		I_{IN}	V_{OS}=V_{CC} or GND, V_{IN}=V_{IH} or V_{IL}	V_{CC}=3V, V_{EE}= GND			±0.25	μA
				V_{CC}=3V, V_{EE}= -3V			±0.5	μA
Control input current		I_{IN}	V_{IN}= V_{CC} or GND	V_{CC}=6V, V_{EE}=GND			±0.1	μA

■ AC ELECTRICAL CHARACTERISTICS

(Input t_R/t_F =3ns, GND=0V, C_L=50pF, unless otherwise specified)

See Fig. 1, Fig. 2 and Fig. 3 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase difference between input and output	t_{PLH} / t_{PHL}	V_{CC}=2V, V_{EE}=GND		3.2	6.0	ns
		V_{CC}=3V, V_{EE}=GND		1.8	3.0	ns
		V_{CC}=4.5V, V_{EE}=GND		1.3	1.8	ns
		V_{CC}=3V, V_{EE}=-3V		1.1	1.3	ns
Output enable time (Note 1)	t_{PZL} / t_{PZH}	V_{CC}=2V, V_{EE}=GND		9	17	ns
		V_{CC}=3V, V_{EE}=GND		5.7	9	ns
		V_{CC}=4.5V, V_{EE}=GND		4.5	6	ns
		V_{CC}=3V, V_{EE}=-3V		5.8	8	ns
Output disable time (Note 1)	t_{PLZ} / t_{PHZ}	V_{CC}=2V, V_{EE}=GND		13.5	21	ns
		V_{CC}=3V, V_{EE}=GND		11.3	15	ns
		V_{CC}=4.5V, V_{EE}=GND		10.3	12	ns
		V_{CC}=3V, V_{EE}=-3V		10.9	13	ns
Control input capacitance (Note 2)	C_{IN}			5	10	pF
COMMON terminal capacitance (Note 2)	C_{IS}	V_{CC}=3V, V_{EE}=-3V		7	15	pF
SWITCH terminal capacitance (Note 2)	C_{OS}	V_{CC}=3V, V_{EE}=-3V		6	13	pF
Feedthrough capacitance (Note 2)	C_{IOS}	V_{CC}=3V, V_{EE}=-3V		3	6	pF
Power dissipation capacitance (Note 3)	C_{PD}	V_{CC}=6V, V_{EE}=GND		18		pF

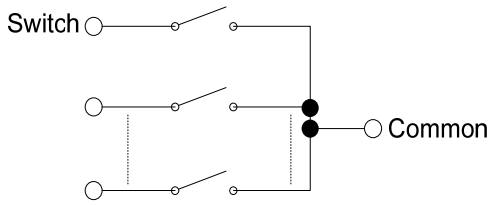
Note: 1. R_L=1k

2. C_{IN}, C_{IS}, C_{OS} and C_{IOS} are guaranteed by the design.
3. CPD is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
   Average operating current can be obtained by the equation.
   $I_{CC}(OPR)=C_{PD}\times V_{CC}\times f_{IN}+V_{CC}$

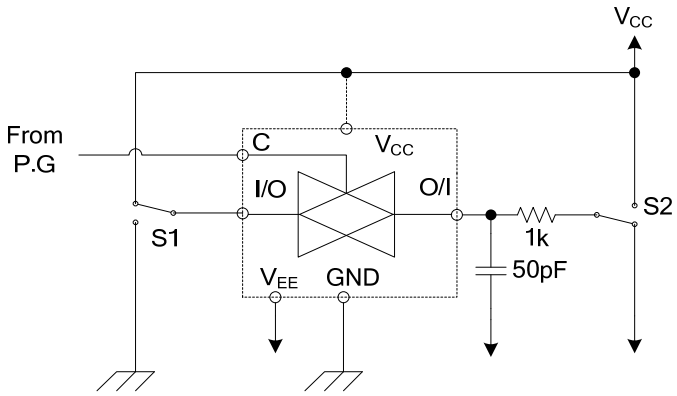
■ ANALOG SWITCH CHARACTERISTICS (GND=0V, unless otherwise specified) (Note)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Sine Wave Distortion	THD	R_L=10k, C_L=50pF, f_{IN}=1k	V_{IN}=2Vp-p, V_{CC}=3V, V_{EE}=0V		0.1		%
			V_{IN}=4Vp-p, V_{CC}=4.5V, V_{EE}=0V		0.03		%
			V_{IN}=6Vp-p, V_{CC}=3V, V_{EE}=-0.3V		0.02		%
Frequency response (switch on)	f_{MAX}	Adjust fIN voltage to obtain 0dBm at V_{OS}. Increase fin frequency until dB meter reads -3dB. R_L=50Ω,C_L=10pF, f_{IN}=1MHz, sine wave (Figure 4)	V_{CC}=3V, V_{EE}=0V		200		MHz
			V_{CC}=4.5V, V_{EE}=0V		200		MHz
			V_{CC}=3V, V_{EE}=-3V		200		MHz
Feed through attenuation (switch off)		V_{IN} is centered at (V_{CC}-V_{EE})/2. Adjust input for 0dBm. R_L=600Ω,C_L=50pF,f_{IN}=1MHz, sine wave (Figure 5)	V_{CC}=3V, V_{EE}=0V		-45		dB
			V_{CC}=4.5V, V_{EE}=0V		-45		dB
			V_{CC}=3V, V_{EE}=-3V		-45		dB
		R_L=50Ω,C_L=10pF,f_{IN}=1MHz, sine wave	V_{CC}=3V, V_{EE}=0V		-60		dB
			V_{CC}=4.5V, V_{EE}=0V		-60		dB
			V_{CC}=3V, V_{EE}=-3V		-60		dB
Crosstalk (control input to signal output)		R_L=600Ω,C_L=50pF,f_{IN}=1MHz, square wave(t_r=t_f=6ns) (Figure 6)	V_{CC}=3V, V_{EE}=0V		90		mV
			V_{CC}=4.5V, V_{EE}=0V		150		mV
			V_{CC}=3V, V_{EE}=-3V		120		mV
Crosstalk (between any switches)		Adjust V_{IN} to obtain 0dBm at input. R_L=600Ω,C_L=50pF,f_{IN}=1MHz, sine wave (Figure 7)	V_{CC}=3V, V_{EE}=0V		-45		dB
			V_{CC}=4.5V, V_{EE}=0V		-45		dB
			V_{CC}=3V, V_{EE}=-3V		-45		dB

Note: These characteristics are determined by design of devices.



■ TEST CIRCUIT AND WAVEFORMS



TEST	S1	S2
t_{PLH}/t_{PHL}	pulse	Open
t_{PHZ}/t_{PZH}	V_{CC}	GND
t_{PLZ}/t_{PZL}	GND	V_{CC}

Fig. 1 Load circuitry for switching times.

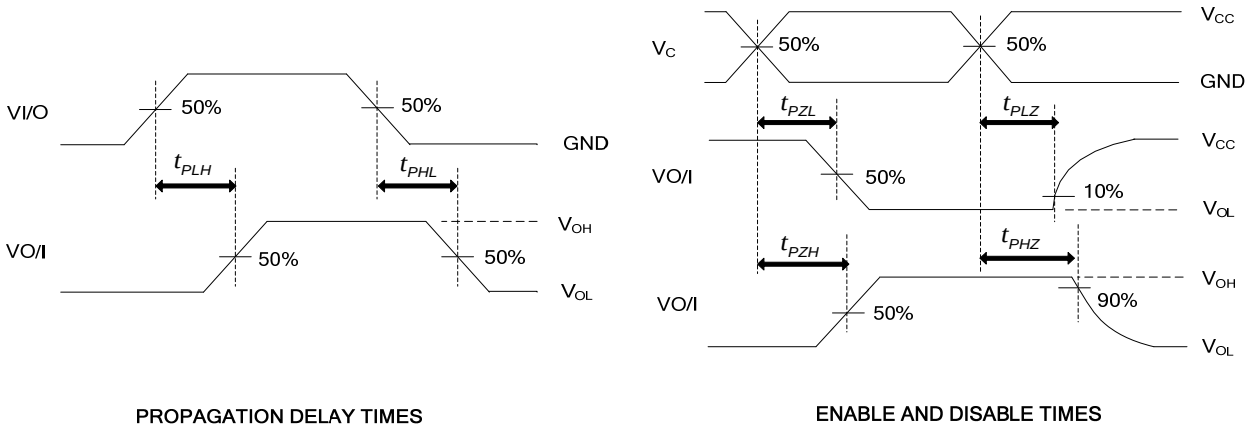


Fig. 2 Propagation delay from input to output and enable, disable times.

■ AC TEST CIRCUIT

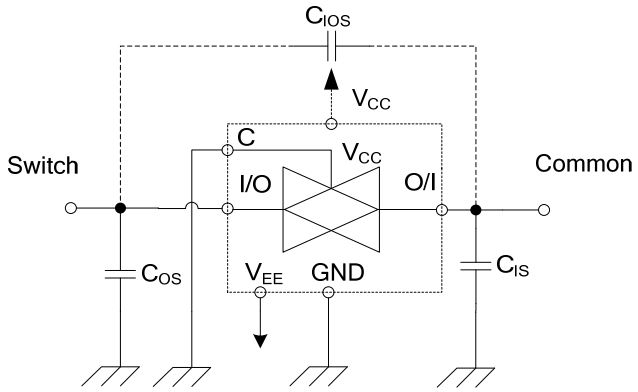


Fig. 3 C_{IOS}, C_{IS}, C_{OS}

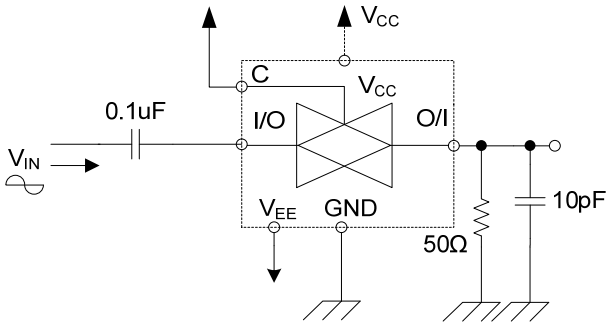


Fig. 4 Frequency Response (switch on)

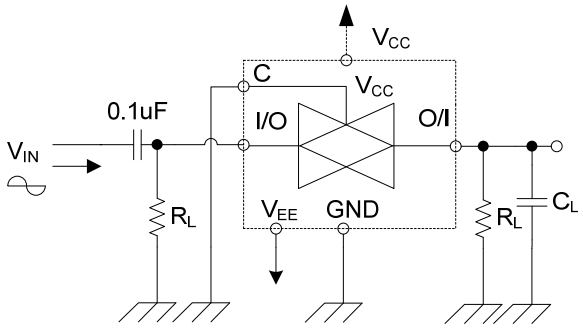


Fig. 5 Feedthrough

■ AC TEST CIRCUIT (Cont.)

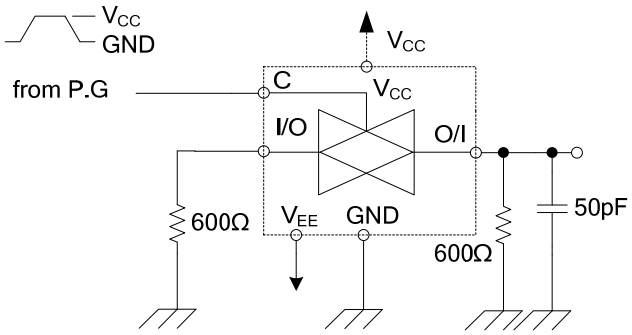


Fig. 6 Cross Talk (control input to output signal)

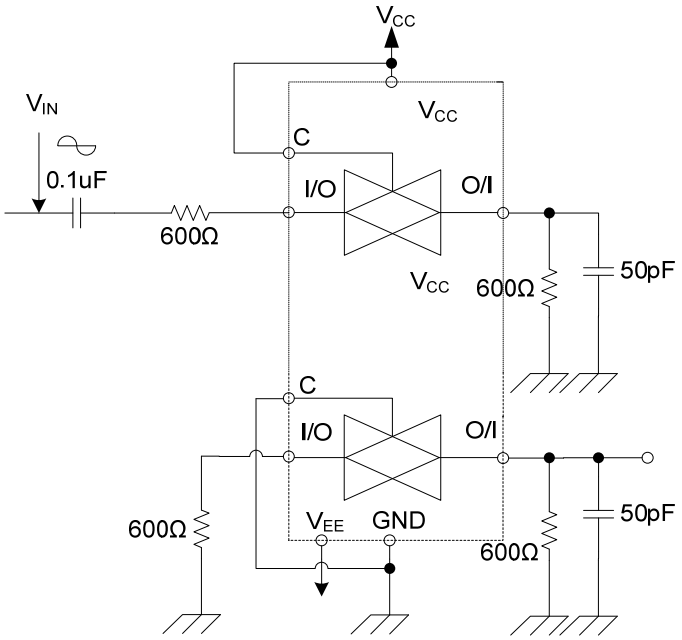


Fig. 7 Cross Talk (between any two switches)