



11N65K-MT

Preliminary

Power MOSFET

11A, 650V N-CHANNEL POWER MOSFET

DESCRIPTION

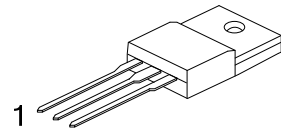
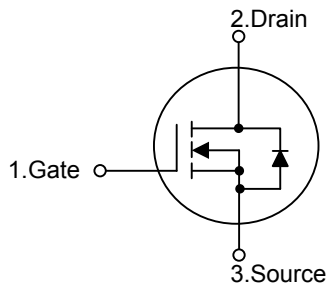
The **UTC 11N65K-MT** is an N-channel enhancement mode power MOSFET. It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance. It also can withstand high energy pulse in the avalanche and commutation mode.

The **UTC 11N65K-MT** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

FEATURES

- * $R_{DS(ON)} < 1.00\Omega$ @ $V_{GS} = 10V$, $I_D = 5.5A$
- * Fast Switching
- * With 100% Avalanche Tested

SYMBOL



TO-220F2

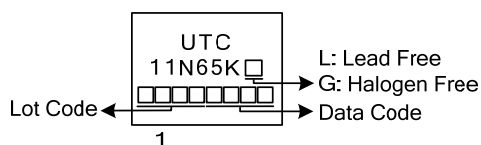
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
11N65KL-TF2-T	11N65KG-TF2-T	TO-220F2	G	D	S	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

<p>11N65KL-TF2-T</p> <p>(1) Packing Type (2) Package Type (3) Green Package</p>		<p>(1) T: Tube (2) TF2: TO-220F2 (3) L: Lead Free, G: Halogen Free and Lead Free</p>
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MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain to Source Voltage	V_{DSS}	650	V
Gate to Source Voltage	V_{GSS}	± 30	V
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$ 11 (Note 2)	A
		$T_C=100^\circ\text{C}$ 7 (Note 2)	A
Pulsed Drain Current (Note 3)	I_{DM}	44 (Note 2)	A
Single Pulsed Avalanche Energy (Note 4)	E_{AS}	440	mJ
Peak Diode Recovery dv/dt (Note 5)	dv/dt	4.5	V/ns
Power Dissipation	P_D	48	W
Derate above 25°C		0.38	W/ $^\circ\text{C}$
Junction Temperature	T_J	+150	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Drain current limited by maximum junction temperature

3. Repetitive Rating : Pulse width limited by maximum junction temperature

4. $L=7.27\text{mH}$, $I_{AS}=11\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$

5. $I_{SD} \leq 11\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	62.5	$^\circ\text{C}/\text{W}$
Junction to Case	θ_{JC}	2.58	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS (T_C=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	650			V
Breakdown Voltage Temperature Coefficient	ΔBV _{DSS} /ΔT _J	I _D =250μA, Referenced to 25°C		0.5		V/°C
Drain-Source Leakage Current	I _{DSS}	V _{DS} =650V, V _{GS} =0V			10	μA
		V _{DS} =650V, T _J =125°C			100	μA
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V ,V _{GS} =±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250μA	2.0		4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =5.5A			1.00	Ω
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz		850	1200	pF
Output Capacitance	C _{OSS}			139	150	pF
Reverse Transfer Capacitance	C _{RSS}			10	20	pF
SWITCHING PARAMETERS						
Total Gate Charge	Q _G	V _{DS} =30V, V _{GS} =10V, I _D =0.5A (Note 1, 2)		35	55	nC
Gate-Source Charge	Q _{GS}			10		nC
Gate-Drain Charge	Q _{GD}			9		nC
Turn-ON Delay Time	t _{D(ON)}	V _{DD} =50V, I _D =1.3A, R _G =3Ω (Note 1, 2)		74	90	ns
Turn-ON Rise Time	t _R			95	120	ns
Turn-OFF Delay Time	t _{D(OFF)}			180	200	ns
Turn-OFF Fall Time	t _F			96	120	ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				11	A
Maximum Body-Diode Pulsed Current	I _{SM}				44	A
Drain-Source Diode Forward Voltage	V _{SD}	I _S =11A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time	t _{rr}	V _{GS} =0V, I _S =11A,		90		ns
Body Diode Reverse Recovery Charge	Q _{RR}	dl _F /dt=100A/μs (Note 1)		1.5		μC

Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%

2. Essentially independent of operating temperature

D.U.T.

V_{DS}

V_{GS}

R_G

Driver

Same Type as D.U.T.

L

V_{DD}

- * dv/dt controlled by R_G
- * I_{SD} controlled by pulse period
- * D.U.T.-Device Under Test

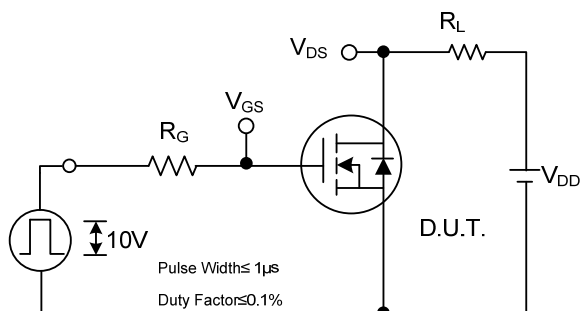
The diagram illustrates the timing relationships for a MOSFET switching event, showing three waveforms: V_{GS} (Driver), I_{SD} (D.U.T.), and V_{DS} (D.U.T.).

- V_{GS} (Driver):** A square wave pulse. The pulse width is labeled **P.W.** and the period is labeled **Period**. The duty cycle is given by $D = \frac{P.W.}{Period}$. The peak voltage is $V_{GS} = 10V$.
- I_{SD} (D.U.T.):** The source-drain current. During the **Body Diode Forward Current** phase, it is labeled I_{FM} . During the **Body Diode Reverse Current** phase, it is labeled I_{RM} . The reverse current is shown as a negative pulse with a slope labeled di/dt .
- V_{DS} (D.U.T.):** The drain-source voltage. It shows a ramp-up during the forward current phase, a flat region during the reverse current phase, and a ramp-down during the reverse current phase. The reverse recovery voltage is labeled **Body Diode Recovery dv/dt** . The peak voltage is V_{DD} .

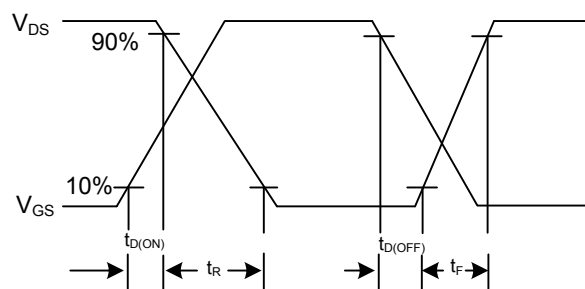
Labels at the bottom indicate the **Body Diode** and **Forward Voltage Drop** regions.

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QW-R205-018.d

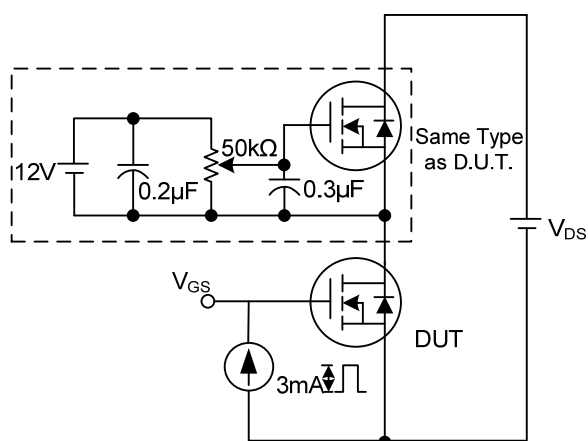
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



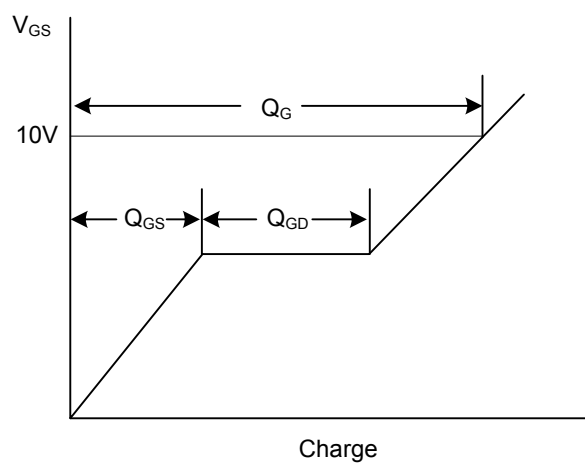
Switching Test Circuit



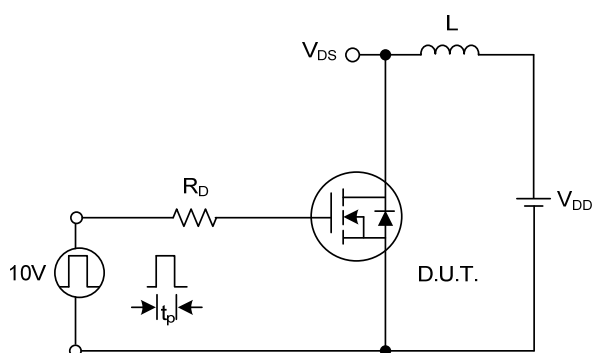
Switching Waveforms



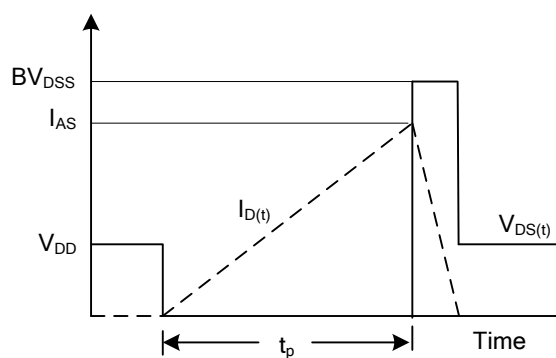
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

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