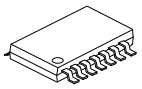
ALDR632

CMOS IC

DIRECT 2-VRMS AUDIO LINE DRIVER WITH ADJUSTABLE GAIN



TSSOP-14

■ DESCRIPTION

The UTC **ALDR632** is a pop-free stereo line driver with the integrated charge pump generating the negative supply rail which allows the removal of the output DC-blocking capacitors. The UTC **ALDR632** provides a clean, pop-free ground-biased audio signal. The UTC **ALDR632** is capable of driving 2VRMS into a 10kΩ load with 3.3V supply voltage. The device has differential inputs and uses external resistors for flexible gain setting. Gain can be configured individually for each channel.

The UTC **ALDR632** has built-in active-mute control for pop-free audio on/off control. The UTC **ALDR632** has an external under-voltage detector that mutes the output when monitored voltage drop below set value.

The device has differential inputs and uses external gain-setting resistors to support a gain range of ±1V/V to ±10V/V, and gain can be configured individually for each channel. Line outputs have ±8-Kv (HBM) IEC ESD protection, requiring just a simple resistor-capacitor ESD protection circuit.

Using the UTC **ALDR632** in audio products can reduce component count considerably compared to traditional headphone amplifiers.

■ FEATURES

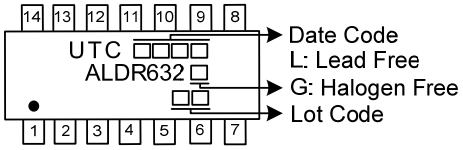
* Low THD+N<0.01% at 2Vrms Into 10kΩ
* Stereo Direct Audio Line driver
  2Vrms Into 10KΩ With 3.3V Supply
* Integrated Charge Pump Generates Negative Supply Rail
* High SNR, >90dB
* Ground-Referenced Outputs Eliminate DC-Blocking Capacitors
* Differential Input and Single-Ended Output
* Adjustable Gain by External Gain-Setting Resistors
* Pop-Free Under-Voltage Protection
* Short-Circuit Protection
* Click- and Pop-Reduction Circuitry
* Active Mute Control for Pop-Free Audio On/Off Control

■ ORDERING INFORMATION

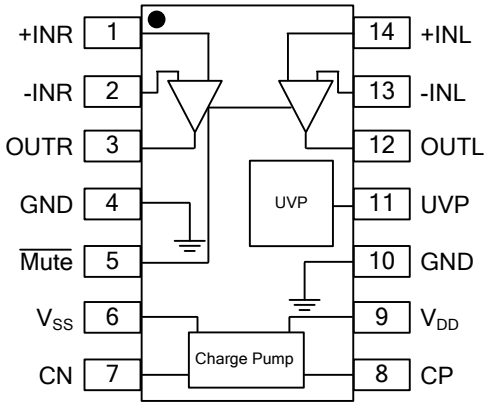
Ordering Number		Package	Packing
Lead Free	Halogen Free		
ALDR632L-P14-R	ALDR632G-P14-R	TSSOP-14	Tape Reel

ALDR632G-P14-R (1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) P14: TSSOP-14 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



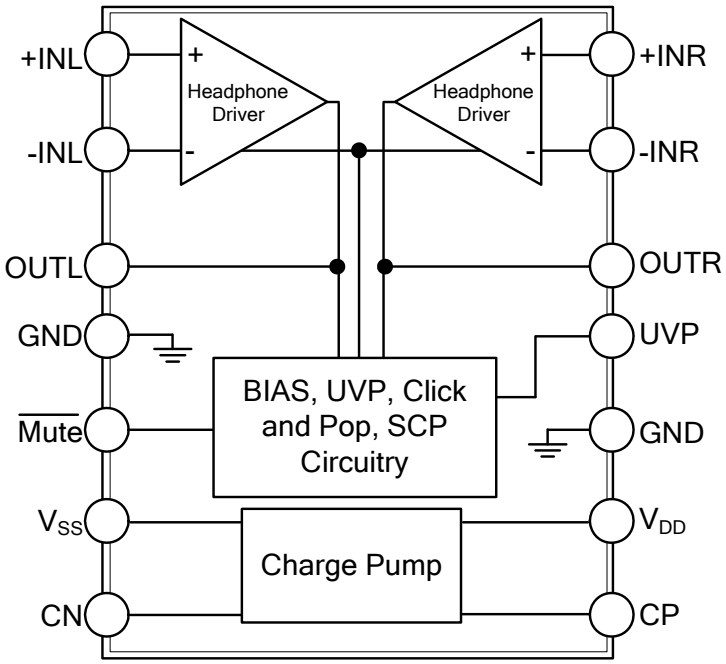
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	+INR	Right-channel OPAMP positive input
2	-INR	Right-channel OPAMP negative input
3	OUTR	Right-channel OPAMP output
4, 10	GND	Ground
5	Mute	Mute, active-low
6	V_{SS}	Supply voltage
7	CN	Charge-pump flying capacitor negative connection
8	CP	Charge-pump flying capacitor positive connection
9	V_{DD}	Positive supply
11	UVP	Under-voltage protection; internal pull-up, unconnected if UVP function is unused.
12	OUTL	Left-channel OPAMP output
13	-INL	Left-channel OPAMP negative input
14	+INL	Left-channel OPAMP positive input

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (over operating free-air temperature range, unless otherwise noted)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply voltage, V_{DD} to GND		-0.3 ~ 4	V
Input Voltage	V_I	V_{SS}-0.3 ~ V_{DD}+0.3	V
Minimum Load Impedance-Line Outputs-OUTL, OUTR	R_L	600	Ω
Mute to GND, UVP to GND		-0.3 ~ V_{DD}+0.3	V
Maximum Operating Junction Temperature Range	T_J	-40 ~ +150	°C
Storage Temperature Range	T_{STG}	-40 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	130	°C/W
Junction to Case	θ_{JC}	49	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply	V_{DD}	DC supply voltage	3	3.3	3.6	V
Load Impedance	R_L		0.6	10		kΩ
Low-Level Input Voltage	V_{IL}	$\overline{\text{Mute}}$		40		%V_{DD}
High-Level Input Voltage	V_{IH}	$\overline{\text{Mute}}$		60		%V_{DD}
Ambient Temperature	T_A		-40	+25	+85	°C

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, Charge pump: C_P=1μF, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Offset Voltage	$\lvert V_{OS}\rvert$	V_{DD}=3.3V		0.5	1	mV
Power-Supply Rejection Ratio	PSRR			80		dB
High-Level Output Voltage	V_{OH}	V_{DD}=3.3V	3.1			V
Low-Level Output Voltage	V_{OL}	V_{DD}=3.3V			-3.05	V
External UVP Detect Voltage	V_{UVP_EX}			1.25		V
External UVP Detect Hysteresis Current	$V_{UVP\_EX\_HYSTERESIS}$			5		μA
Charge-Pump Switching Frequency	f_{CP}		200	300	400	kHz
High-Level Input Current, $\overline{\text{Mute}}$	$\lvert I_{IH}\rvert$	V_{DD}=3.3V, V_{IH}=V_{DD}			1	μA
Low-Level Input Current, $\overline{\text{Mute}}$	$\lvert I_{IL}\rvert$	V_{DD}=3.3V, V_{IL}=0V			1	μA
Supply Current	I_{DD}	V_{DD}=3.3V, no load, $\overline{\text{Mute}}$ =V_{DD}	5	14	25	mA
		V_{DD}=3.3V, no load, $\overline{\text{Mute}}$ =GND, disabled		1		mA

■ OPERATING CHARACTERISTICS

(V_{DD}=3.3V, R_{DL}=10kΩ, R_{FB}=30kΩ, R_{IN}=15kΩ, T_A=25°C, Charge pump: C_P=1μF, unless otherwise noted))

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage, Outputs in Phase	V_O	THD+N=1%, V_{DD}=3.3V, f=1kHz, R_L=10KΩ	2	2.4		Vrms
Total Harmonic Distortion Plus Noise	THD+N	V_O=2 V_{RMS}, f=1kHz		0.002		%
Signal-to-Noise Ratio (Note 1)	SNR	A-weighted		105		dB
Dynamic Range	DNR	A-weighted		105		dB
Noise Voltage	V_N	A-weighted		11		μV
Output Impedance When Muted	Z_O	$\overline{\text{Mute}}$ =GND		100		Ω
Input-to-Output Attenuation When Muted		$\overline{\text{Mute}}$ =GND		80		dB
Crosstalk-L to R, R to L		V_O=1 V_{RMS}		-110		dB
Current Limit	I_{LIMIT}	PV_{DD}=3.3V		25		mA

Note: SNR is calculated relative to 2 V_{RMS} output.

■ APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 1 illustrates the conventional line-driver amplifier connection to the load and output signal. DC blocking capacitors are often large in value. The line load (typical resistive values of 600Ω~10kΩ) combines with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (CO), and the cutoff frequency (f_C).

$$f_C = \frac{1}{2\pi R_L C_O} \quad (1)$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_C} \quad (2)$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

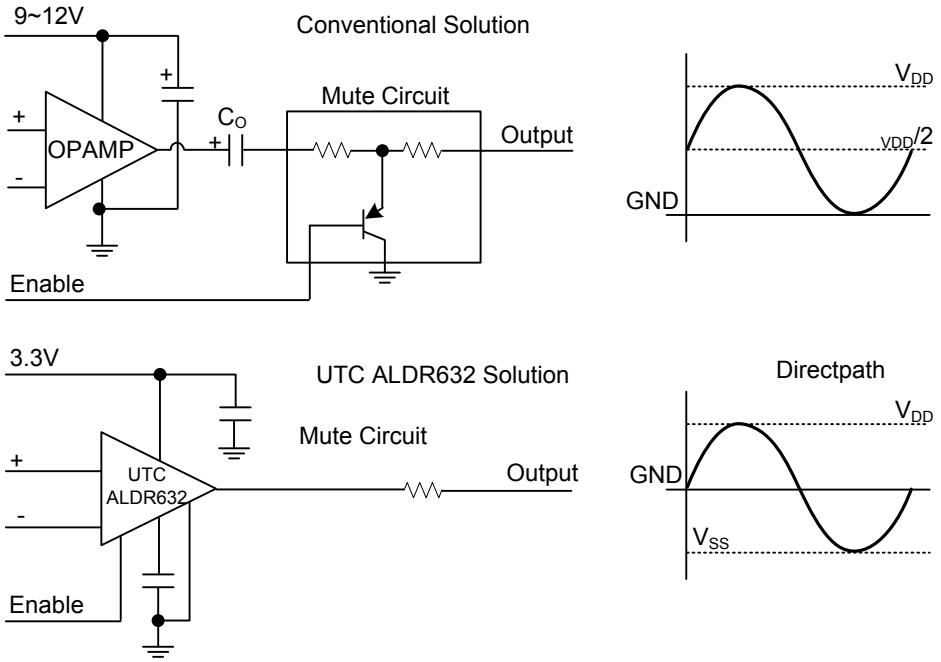


Figure 1. Conventional and DirectPath Line Drivers

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split-supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath amplifier requires no output dc blocking capacitors. The bottom block diagram and waveform of Figure 1 illustrate the ground-referenced line-driver architecture. This is the architecture of the UTC **ALDR632**.

■ APPLICATION INFORMATION (Cont.)

GAIN-SETTING RESISTOR RANGES

The gain-setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability, and input capacitor size of the UTC **ALDR632** are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Table 1. Recommended Resistor Values

GAIN	INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}
-1V/V	10kΩ	10kΩ
-1.5V/V	8.2kΩ	12kΩ
-2V/V	15kΩ	30kΩ
-10V/V	4.7kΩ	47kΩ

UTC ALDR632 UVP OPERATION

The shutdown threshold at the UVP pin is 1.25V. The customer must use a resistor divider to obtain the shutdown threshold and hysteresis desired for a particular application. The customer-selected thresholds can be determined as follows:

EXTERNAL UNDERVOLTAGE DETECTION

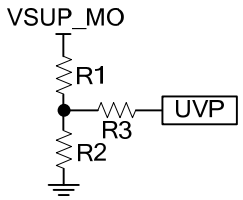
External undervoltage detection can be used to mute/shut down the UTC **ALDR632** before an input device can generate a pop.

The shutdown threshold at the UVP pin is 1.25V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application. The thresholds can be determined as follows:

V_{UVP}=(1.25–6μA×R3)×(R1+R2)/R2

Hysteresis=5μA×R3×(R1+R2)/R2

For example, to obtain V_{UVP}=3.8V and 1-V hysteresis, we can use R1=3kΩ, R2=1kΩ, and R3=50kΩ.



INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the **ALDR632**. These capacitors block the dc portion of the audio source and allow the UTC **ALDR632** inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

It is recommended to use electrolytic capacitors or high-voltage-rated capacitors as input blocking capacitors to ensure minimal variation in capacitance with input voltages. Such variation in capacitance with input voltages is commonly seen in ceramic capacitors and can increase low-frequency audio distortion.

$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi f_{CIN} R_{IN}} \quad (3)$$

■ APPLICATION INFORMATION (Cont.)

CHARGE-PUMP FLYING CAPACITOR AND PVSS CAPACITOR

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge-pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1μF is typical. Capacitor values that are smaller than 1μF can be used, but the maximum output voltage may be reduced and the device may not operate to specifications. If the UTC **ALDR632** is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the V_{DD} connection.

DECOUPLING CAPACITORS

The UTC **ALDR632** is a DirectPath line-driver amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good, low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the UTC **ALDR632** is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

USING THE UTC ALDR632 AS A SECOND-ORDER FILTER

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the UTC **ALDR632**, as it can be used like a standard operational amplifier. Several filter topologies can be implemented, both single-ended and differential. In Figure 2, multi-feedback (MFB) with differential input and single-ended input are shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc gain to 1, helping to reduce the output dc offset to a minimum.

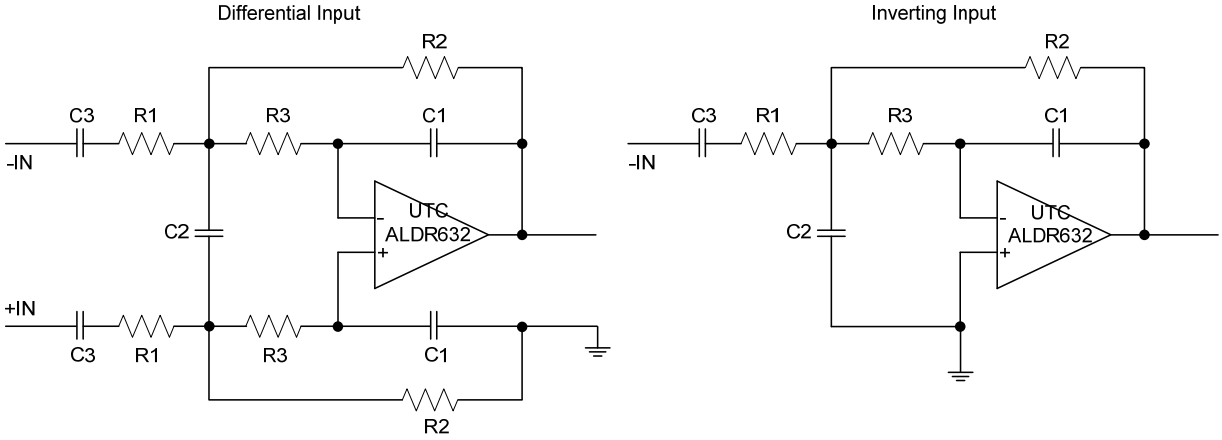


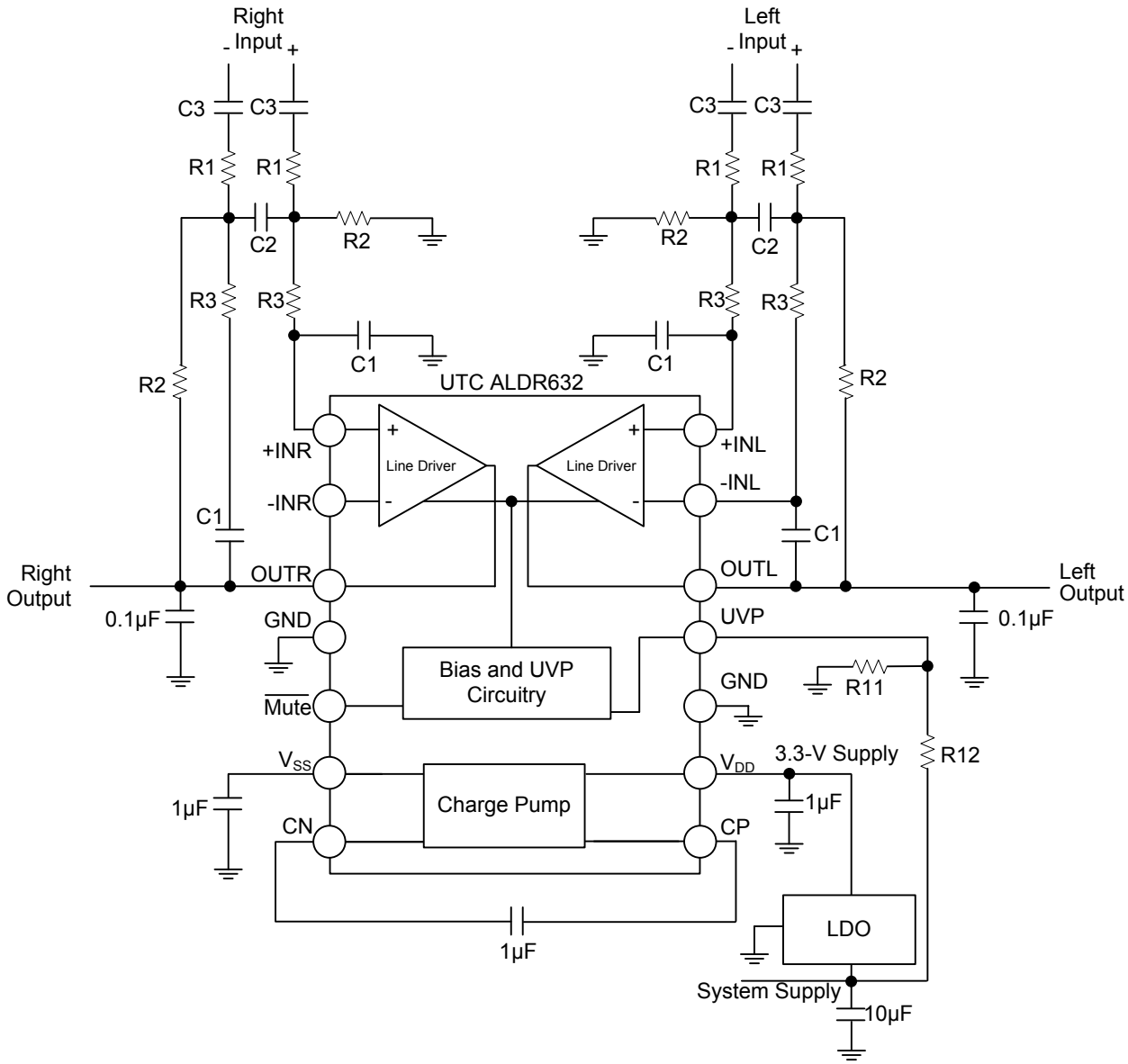
Figure 2. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small-size ac-coupling capacitor. With the proposed values of R1=15kΩ, R2=30kΩ, and R3=43kΩ, a dynamic range (DYR) of 106dB can be achieved with a 1-μF input ac-coupling capacitor.

GAIN-SETTING RESISTORS

The gain-setting resistors, R_{IN} and R_{fb}, respectively, to minimize capacitive loading on these input pins and to ensure maximum stability of the UTC **ALDR632**.

■ TYPICAL APPLICATION CIRCUIT



R1=15kΩ, R2=30kΩ, R3=43kΩ, C1=47pF, C2=180pF
Differential-input, single-ended output, second-order filter