



ULC3702

CMOS IC

DUAL MICROPOWER CMOS VOLTAGE COMPARATORS

DESCRIPTION

The UTC **ULC3702** consists of two independent micropower voltage comparators designed to operate from a single supply and be compatible with modern HCMOS logic systems. The push-pull CMOS output stage drives capacitive loads directly without a power-consuming pull up resistor to achieve the stated response time. Eliminating the pull up resistor not only reduces power dissipation, but also saves board space and component cost. The output stage is also fully compatible with TTL requirements.

FEATURES

- * Push-Pull CMOS Output Drives Capacitive Loads Without Pull up Resistor
- * Fast Response Time $t_{PLH}=2.7\mu s$ (Typ.) With 5-mV Overdrive
- * Single-Supply Operation: 3V ~ 16V

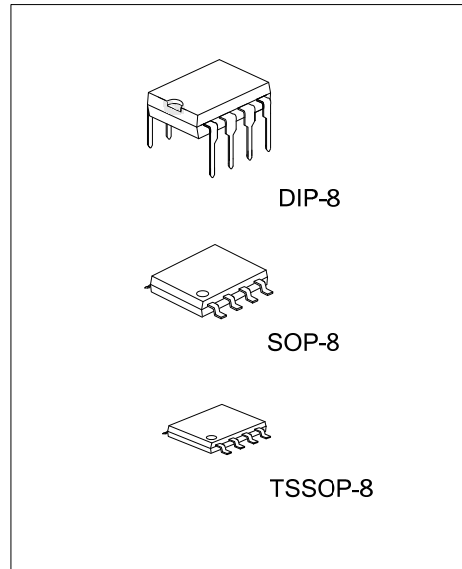
ORDERING INFORMATION

| Ordering Number | | Package | Packing |
|-----------------|----------------|---------|-----------|
| Lead Free | Halogen Free | | |
| ULC3702L-D08-T | ULC3702G-D08-T | DIP-8 | Tube |
| ULC3702L-S08-R | ULC3702G-S08-R | SOP-8 | Tape Reel |
| ULC3702L-P08-R | ULC3702G-P08-R | TSSOP-8 | Tape Reel |

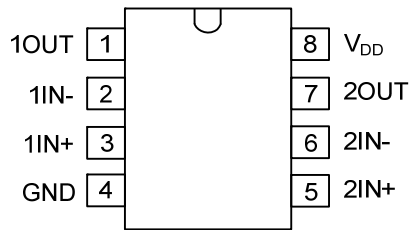
| | |
|--|--|
| <p>ULC3702G-D08-T</p> <ul style="list-style-type: none"> (1)Packing Type (2)Package Type (3)Green Package | <ul style="list-style-type: none"> (1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8, P08: TSSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free |
|--|--|

MARKING

| DIP-8 | SOP-8 | TSSOP-8 |
|---|---|---|
| <p> 8 7 6 5 → Date Code UTC □□□□ L: Lead Free G: Halogen Free □□ → Lot Code 1 2 3 4 </p> | <p> 8 7 6 5 → Date Code UTC □□□□ L: Lead Free G: Halogen Free □□ → Lot Code 1 2 3 4 </p> | <p> 8 → Date Code 7 → L: Lead Free 6 → G: Halogen Free 5 → Lot Code 1 • UTC □□□□ 2 ULC3702 □ 3 □□ 4 </p> |



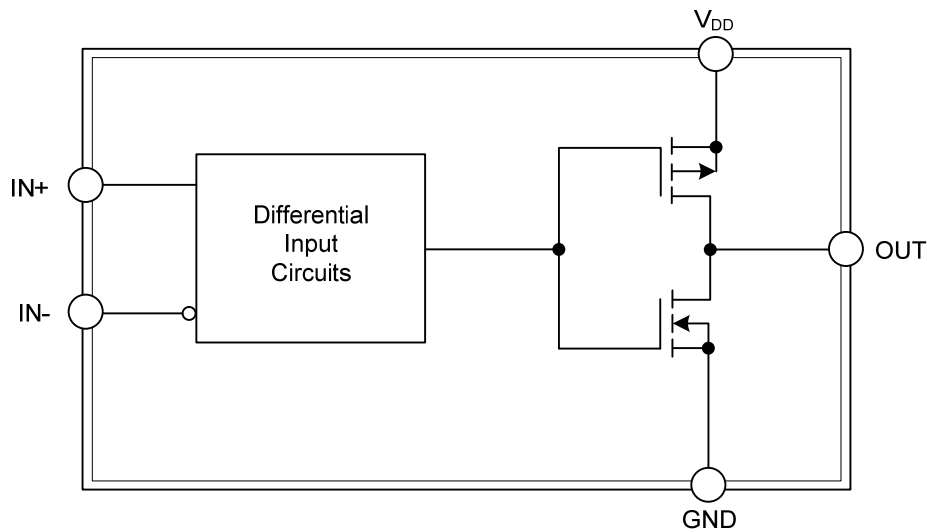
■ PIN CONFIGURATION



■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------|-----------------|-----------------------------------|
| 1 | 1OUT | Channel 1 output pin |
| 2 | 1IN- | Inverting input for channel 1 |
| 3 | 1IN+ | Non-inverting input for channel 1 |
| 4 | GND | Ground |
| 5 | 2IN+ | Non-inverting input for channel 2 |
| 6 | 2IN- | Inverting input for channel 2 |
| 7 | 2OUT | Channel 2 output pin |
| 8 | V _{DD} | Supply voltage |

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|--------------------------------------|-----------|-----------------|------|
| Supply Voltage Range (Note 1) | V_{DD} | -0.3 ~ 18 | V |
| Differential Input Voltage (Note 2) | V_{ID} | ±18 | V |
| Input Voltage Range | V_I | -0.3 ~ V_{DD} | V |
| Output Voltage Range | V_O | -0.3 ~ V_{DD} | V |
| Input Current | I_I | ±5 | mA |
| Output Current (Each Output) | I_O | ±20 | mA |
| Power Dissipation | DIP-8 | 780 | mW |
| | SOP-8 | 420 | mW |
| | TSSOP-8 | 350 | mW |
| Operating Free-Air Temperature Range | T_A | -40 ~ +85 | °C |
| Storage Temperature Range | T_{STG} | -65 ~ +150 | °C |

- Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
 2. All voltage values, except differential voltages, are with respect to network ground.
 3. Differential voltages are at IN+ with respect to IN-.

■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNIT |
|--------------------------------|----------|------|-----|--------------|------|
| Supply Voltage | V_{DD} | 3 | 5 | 16 | V |
| Common-Mode Input Voltage | V_{IC} | -0.2 | | $V_{DD}-1.5$ | V |
| High-Level Output Current | I_{OH} | | | -20 | mA |
| Low-Level Output Current | I_{OL} | | | 20 | mA |
| Operating Free-Air Temperature | T_A | -40 | | +85 | °C |

■ ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $T_A=25^\circ C$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS (Note 1) | MIN | TYP | MAX | UNIT |
|-----------------------------------|-----------|---|------------------|-----|-----|------|
| Input Offset Voltage | V_{IO} | $V_{DD}=5V\sim 10V$, $V_{IC}=V_{ICRmin}$, (Note 2) | | 1.2 | 5 | mV |
| Input Offset Current | I_{IO} | $V_{IC}=2.5V$ | | 1 | | pA |
| Input Bias Current | I_{IB} | $V_{IC}=2.5V$ | | 5 | | pA |
| Common Mode Input Voltage Range | V_{ICR} | | $0\sim V_{DD}-1$ | | | V |
| Common-Mode Rejection Ratio | CMRR | $V_{IC}=V_{ICRmin}$ | | 84 | | dB |
| Supply-Voltage Rejection Ratio | K_{SVR} | $V_{DD}=5V\sim 10V$ | | 85 | | dB |
| High Level Output Voltage | V_{OH} | $V_{ID}=1V$, $I_{OH}=-4mA$ | 4.5 | 4.7 | | V |
| Low Level Output Voltage | V_{OL} | $V_{ID}=-1V$, $I_{OL}=4mA$ | | 210 | 300 | mV |
| Supply Current (Both Comparators) | I_{DD} | Outputs Low, No Load | | 18 | 40 | μA |

- Notes: 1. All characteristics are measured with zero common-mode voltage unless otherwise noted.
 2. The offset voltage limits given are the maximum values required to drive the output up to 4.5 V or down to 0.3 V.

■ SWITCHING CHARACTERISTICS ($V_{DD}=5V$, $T_A=25^\circ C$, unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---|-----------|------------------------|----------------|------|------|---------|---------|
| Propagation Delay Time, Low-to-High-Level Output (Note) | t_{PLH} | $f=10kHz$, $C_L=50pF$ | Overdrive=2mV | | 4.5 | | μs |
| | | | Overdrive=5mV | | 2.7 | | μs |
| | | | Overdrive=10mV | | 1.9 | | μs |
| | | | Overdrive=20mV | | 1.4 | | μs |
| | | | Overdrive=40mV | | 1.1 | | μs |
| Propagation Delay Time, High-to-Low-Level Output (Note) | t_{PHL} | $V_I=1.4V$ Step at IN+ | | 1.1 | | μs | |
| | | $f=10kHz$, $C_L=50pF$ | Overdrive=2mV | | 4 | | μs |
| | | | Overdrive=5mV | | 2.3 | | μs |
| | | | Overdrive=10mV | | 1.5 | | μs |
| | | | Overdrive=20mV | | 0.95 | | μs |
| | | Overdrive=40mV | | 0.65 | | μs | |
| | | $V_I=1.4V$ Step at IN+ | | 0.15 | | μs | |
| Fall Time | t_f | $f=10kHz$, $C_L=50pF$ | Overdrive=50mV | 50 | | ns | |
| Rise Time | t_r | $f=10kHz$, $C_L=50pF$ | Overdrive=50mV | 125 | | ns | |

Note: Simultaneous switching of inputs causes degradation in output response.

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