



## 2NM65-FD

Power MOSFET

### 2A, 650V N-CHANNEL SUPER-JUNCTION MOSFET

#### DESCRIPTION

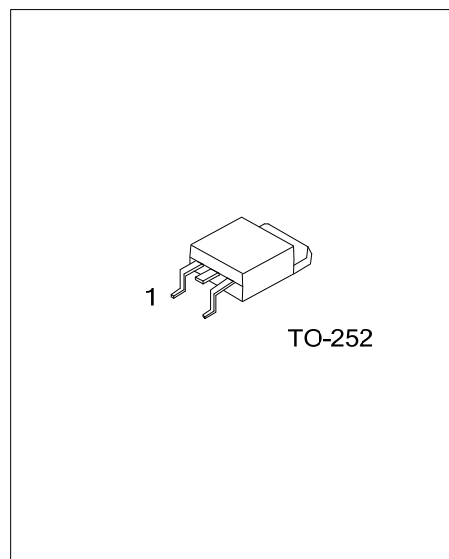
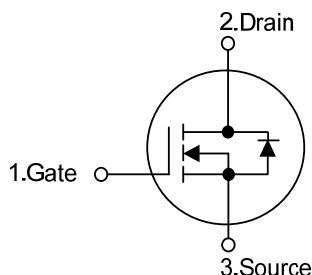
The UTC **2NM65-FD** is a Super Junction MOSFET Structure. It uses UTC advanced planar stripe, DMOS technology to provide customers perfect switching performance, minimal on-state resistance.

The UTC **2NM65-FD** is universally applied in electronic lamp ballasts based on half bridge topology, high efficiency switched mode power supplies, active power factor correction, etc.

#### FEATURES

- \*  $R_{DS(ON)} < 2.6 \Omega$  @  $V_{GS} = 10V$ ,  $I_D = 1.0A$
- \* Fast switching capability
- \* Avalanche energy specified
- \* Improved dv/dt capability, high ruggedness

#### SYMBOL



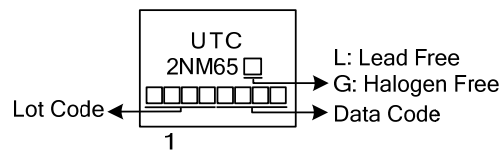
#### ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Lead Free	Halogen Free		1	2	3	
2NM65L-TN3-R	2NM65G-TN3-R	TO-252	G	D	S	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

2NM65G-TN3-R	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) TN3: TO-252
	(3)Green Package	(3) G: Halogen Free and Lead Free L: Lead Free

## ■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		$V_{DS}$	650	V
Gate-Source Voltage		$V_{GS}$	$\pm 30$	V
Drain Current	Continuous	$I_D$	2	A
	Pulsed (Note 2)	$I_{DM}$	6	A
Avalanche Energy	Single Pulsed (Note 3)	$E_{AS}$	72	mJ
Peak Diode Recovery dv/dt (Note 4)		dv/dt	8	V/ns
Power Dissipation		$P_D$	44	W
Junction Temperature		$T_J$	+150	$^\circ\text{C}$
Storage Temperature		$T_{STG}$	-55 ~ +150	$^\circ\text{C}$

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
 2. Repetitive Rating: Pulse width limited by maximum junction temperature.  
 3.  $L=144\text{mH}$ ,  $I_{AS}=1.0\text{A}$ ,  $V_{DD}=50\text{V}$ ,  $R_G=25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$   
 4.  $I_{SD}\leq 2.0\text{A}$ ,  $di/dt\leq 200\text{A}/\mu\text{s}$ ,  $V_{DD}\leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$

■ THERMAL DATA

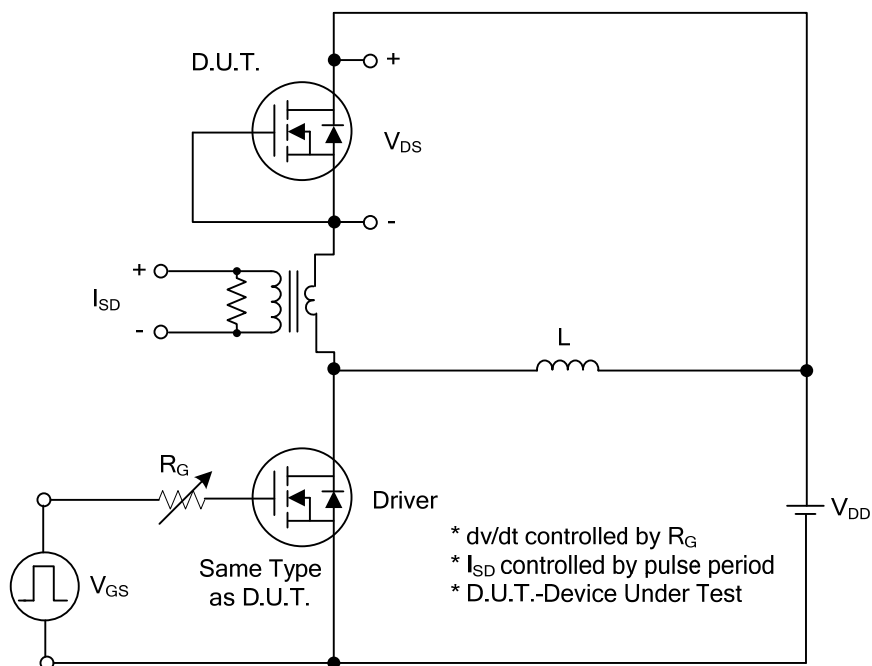
PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		$\theta_{JA}$	100	$^\circ\text{C}/\text{W}$
Junction to Case		$\theta_{JC}$	2.8	$^\circ\text{C}/\text{W}$

■ ELECTRICAL CHARACTERISTICS ( $T_J=25^\circ\text{C}$ , unless otherwise specified)

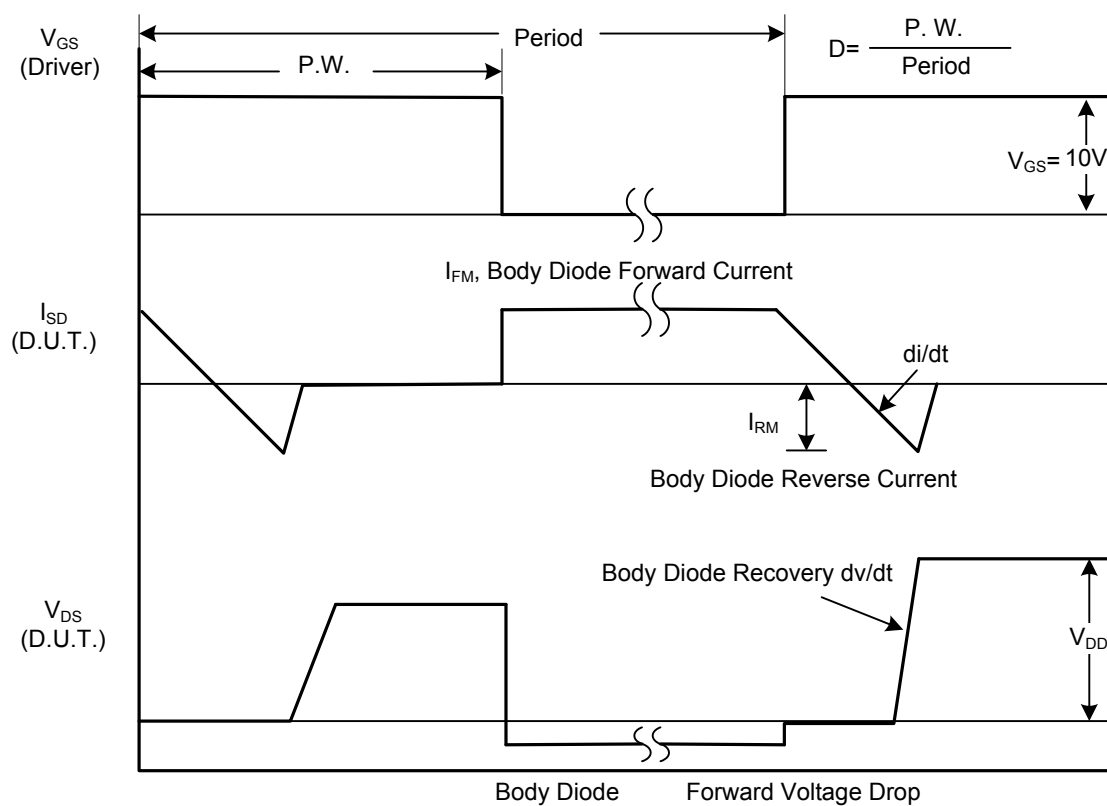
PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	650			V
Drain-Source Leakage Current		I <sub>DSS</sub>	V <sub>DS</sub> = 650V, V <sub>GS</sub> = 0V			10	μA
Gate-Source Leakage Current	Forward	I <sub>GSS</sub>	V <sub>GS</sub> = 30V, V <sub>DS</sub> = 0V			100	nA
	Reverse		V <sub>GS</sub> = -30V, V <sub>DS</sub> = 0V			-100	nA
ON CHARACTERISTICS							
Gate Threshold Voltage		V <sub>GS(TH)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.5		4.5	V
Static Drain-Source On-State Resistance		R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =1.0A			2.6	Ω
DYNAMIC CHARACTERISTICS							
Input Capacitance		C <sub>ISS</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f =1MHz		150		pF
Output Capacitance		C <sub>OSS</sub>			140		pF
Reverse Transfer Capacitance		C <sub>RSS</sub>			12		pF
SWITCHING CHARACTERISTICS							
Turn-On Delay Time (Note 1)		t <sub>D(ON)</sub>	V <sub>DD</sub> =300V, V <sub>GS</sub> =10V, I <sub>D</sub> =2.0A, R <sub>G</sub> =25Ω (Note 1, 2)		1		ns
Turn-On Rise Time		t <sub>R</sub>			9		ns
Turn-Off Delay Time		t <sub>D(OFF)</sub>			18		ns
Turn-Off Fall Time		t <sub>F</sub>			22		ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
Continuous Drain-Source Current		I <sub>S</sub>				2.0	A
Maximum Body-Diode Pulsed Current		I <sub>SM</sub>				6.0	A
Drain-Source Diode Forward Voltage (Note 1)		V <sub>SD</sub>	I <sub>S</sub> =2.0A, V <sub>GS</sub> =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)		t <sub>rr</sub>	I <sub>S</sub> =2.0A, V <sub>GS</sub> =0V		110		nS
Body Diode Reverse Recovery Charge		Q <sub>rr</sub>	dI/dt=100A/μs		0.4		μC

Notes: 1. Pulse Test: Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$ .  
 2. Essentially independent of operating temperature.

# ■ TEST CIRCUITS AND WAVEFORMS

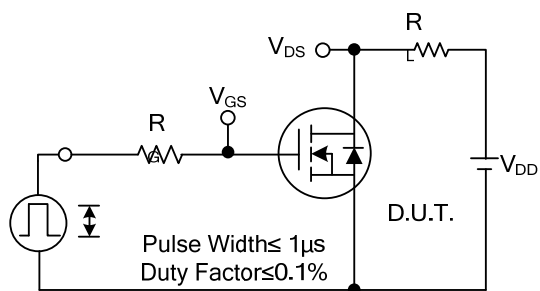


Peak Diode Recovery dv/dt Test Circuit

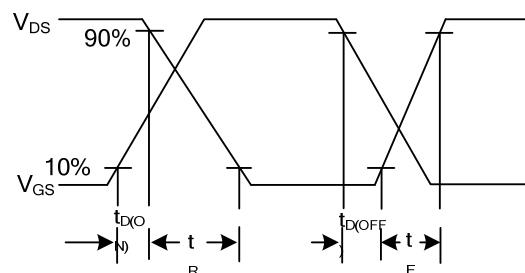


Peak Diode Recovery dv/dt Waveforms

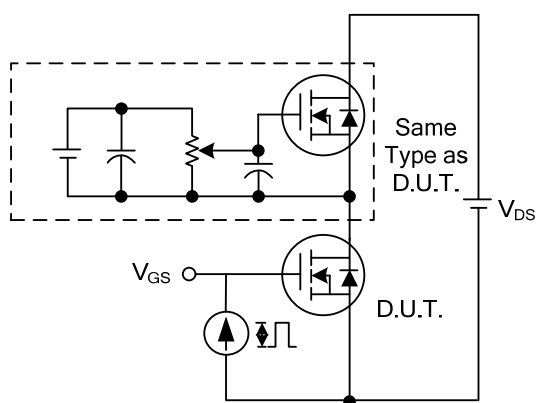
### ■ TEST CIRCUITS AND WAVEFORMS



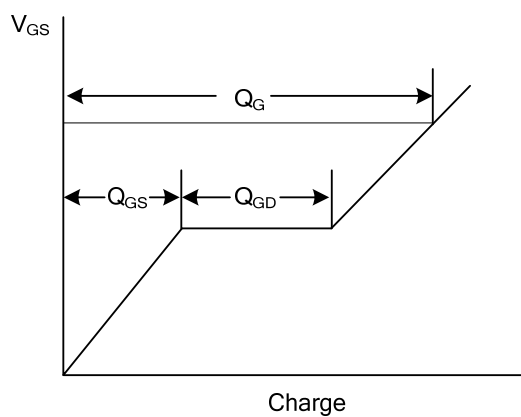
Switching Test Circuit



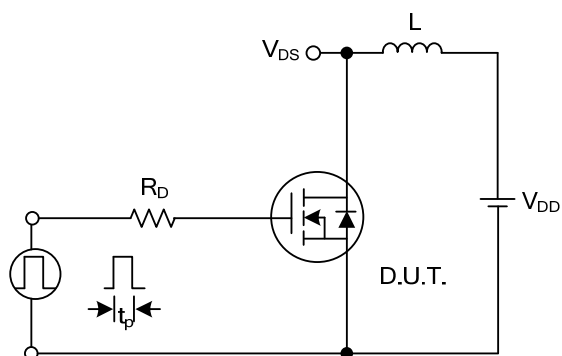
Switching Waveforms



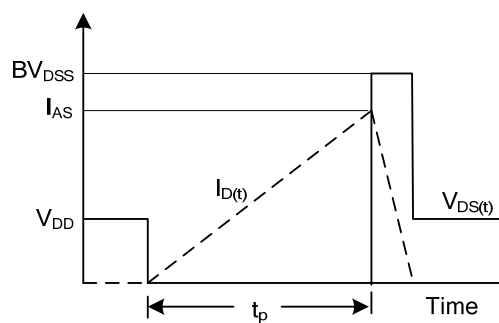
Gate Charge Test Circuit



Gate Charge Waveform

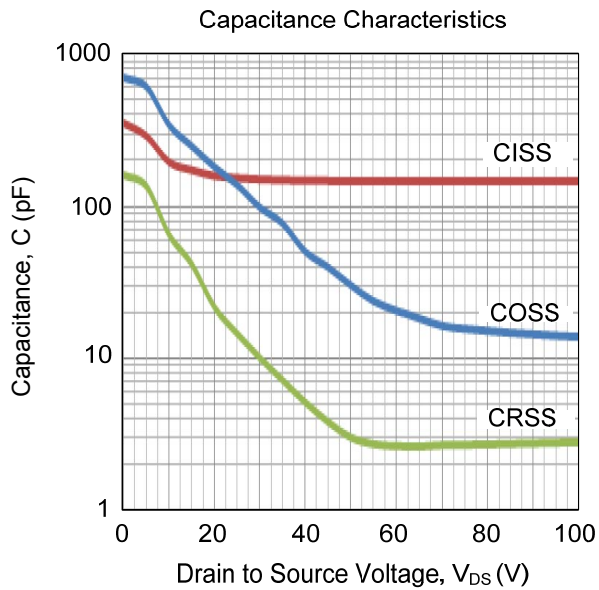


Unclamped Inductive Switching Test Circuit



Unclamped Inductive Switching Waveforms

## ■ TYPICAL CHARACTERISTICS



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