



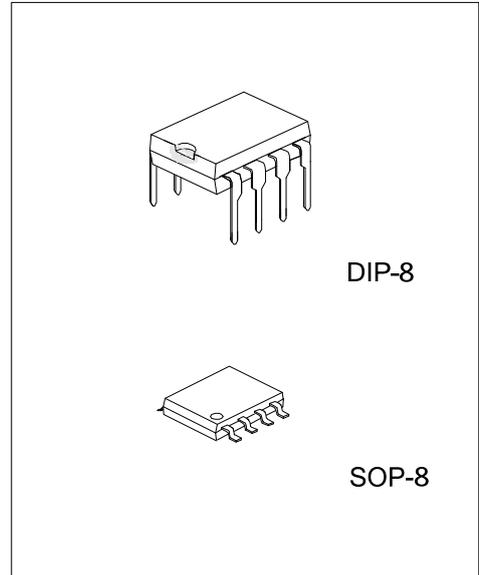
## OP07C

## LINEAR INTEGRATED CIRCUIT

### VERY LOW OFFSET VOLTAGE SINGLE OPERATIONAL AMPLIFIER

#### DESCRIPTION

The **OP07C** offers low offset and long-term stability by means of a low-noise, chopperless, bipolar-input-transistor amplifier circuit. For most applications, external components are not required for offset nulling and frequency compensation. The true differential input, with a wide input-voltage range and outstanding common-mode rejection, provides maximum flexibility and performance in high-noise environments and in noninverting applications. Low bias currents and extremely high input impedances are maintained over the entire temperature range.



#### FEATURES

- \* Low Noise
- \* No External Components Required
- \* Replace Chopper Amplifiers at a Lower Cost
- \* Wide Input-Voltage Range: 0 to  $\pm 14V$  (Typ.)
- \* Wide Supply-Voltage Range:  $\pm 3V$  to  $\pm 18V$

#### ORDERING INFORMATION

Order Number		Package	Packing
Lead Free	Halogen Free		
OP07CL-D08-T	OP07CG-D08-T	DIP-8	Tube
OP07CL-S08-R	OP07CG-S08-R	SOP-8	Tape Reel

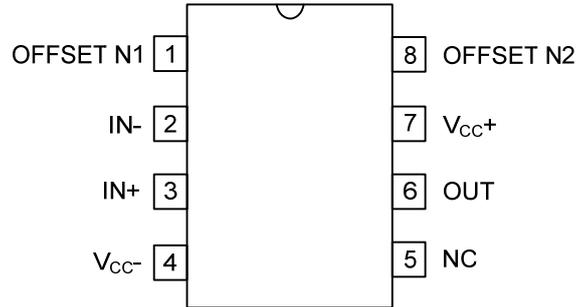
Note: Pin Assignment: G: Gate D: Drain S: Source

<p>OP07CG-D08-T</p> <ul style="list-style-type: none"> <li>(1) Packing Type</li> <li>(2) Package Type</li> <li>(3) Green Package</li> </ul>	<ul style="list-style-type: none"> <li>(1) T: Tube, R: Tape Reel</li> <li>(2) D08: DIP-8, S08: SOP-8</li> <li>(3) G: Halogen Free and Lead Free, L: Lead Free</li> </ul>
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#### MARKING

DIP-8	SOP-8
<p>UTC □□□□ OP07C □</p> <p>1 2 3 4</p>	<p>UTC □□□□ OP07C □</p> <p>1 2 3 4</p>
<p>8 7 6 5 → Date Code</p> <p>L: Lead Free</p> <p>G: Halogen Free</p> <p>□ □ → Lot Code</p>	<p>8 7 6 5 → Date Code</p> <p>L: Lead Free</p> <p>G: Halogen Free</p> <p>□ □ → Lot Code</p>

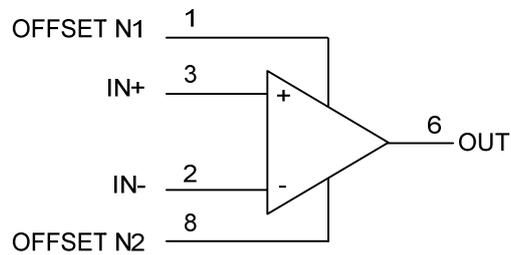
### ■ PIN CONFIGURATION



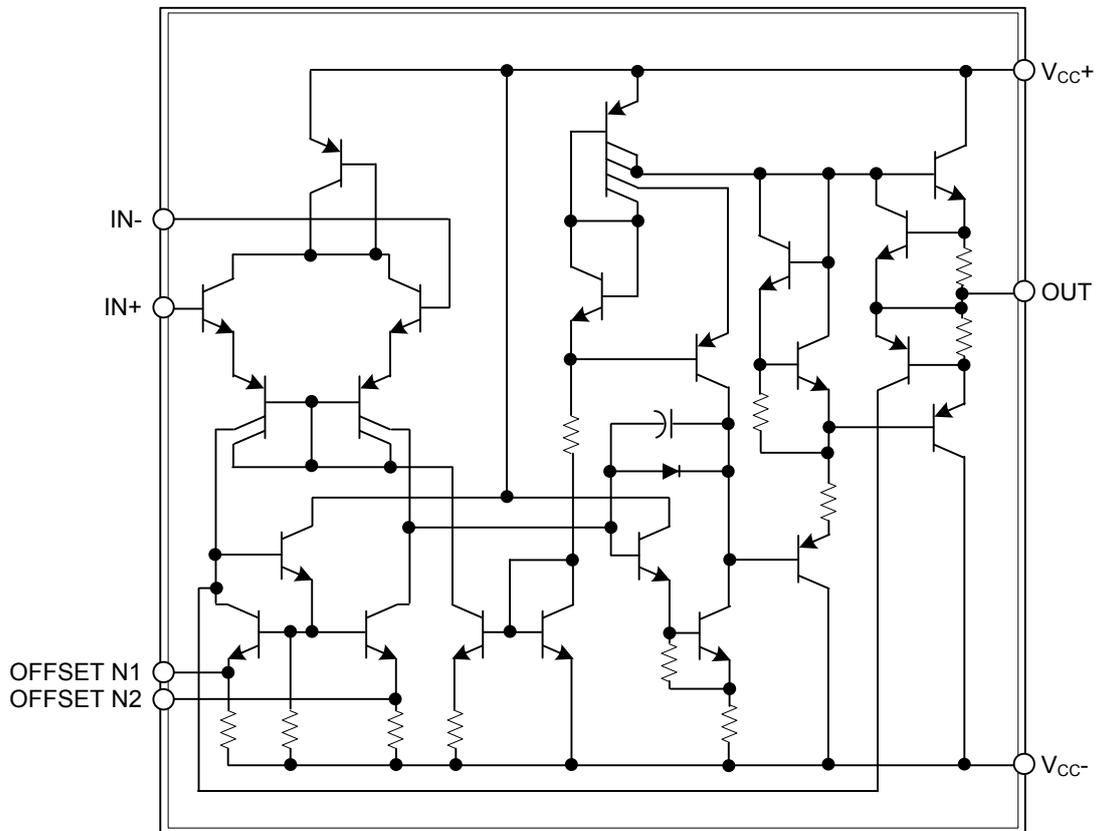
### ■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	OFFSET N1	External input offset voltage adjustment
2	IN-	Inverting input
3	IN+	Noninverting input
4	V <sub>CC-</sub>	Negative supply
5	NC	Do not connect
6	OUT	Output
7	V <sub>CC+</sub>	Positive supply
8	OFFSET N2	External input offset voltage adjustment

### ■ SIMPLIFIED SCHEMATIC



■ BLOCK DIAGRAM



### ■ ABSOLUTE MAXIMUM RATING

(Over operating free-air temperature range unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC+}$	0 ~ 22 (Note 2)	V
	$V_{CC-}$	-22 ~ 0 (Note 2)	V
Differential Input Voltage (Note 3)	$V_{ID}$	±30	V
Input Voltage Range (Either Input) (Note 4)	$V_I$	±22	V
Operating Virtual-Junction Temperature	$T_J$	+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .

3. Differential voltages are at  $IN+$  with respect to  $IN-$ .

4. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.

### ■ RECOMMENDED OPERATING CONDITIONS

(Over operating free-air temperature range unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC+}$	3 ~ 18	V
	$V_{CC-}$	-3 ~ -18	V
Common-Mode Input Voltage ( $V_{CC±} = ±15$ V)	$V_{IC}$	-13 ~ 13	V
Operating Free-Air Temperature	$T_A$	-40 ~ +85	°C

## ■ ELECTRICAL CHARACTERISTICS

(At specified free-air temperature,  $V_{CC} \pm \pm 15V$ , unless otherwise specified) (Note 1)

PARAMETER	SYMBOL	TEST CONDITIONS	$T_A$ (Note 2)	MIN	TYP	MAX	UNIT
Input Offset Voltage	$V_{IO}$	$V_O=0V, R_S=50\Omega$	25°C		60		$\mu V$
			0°C~70°C		85		$\mu V$
Long-Term Drift of Input Offset Voltage		(Note 1)			0.4		$\mu V/mo$
Offset Adjustment Range		$R_S=20k\Omega$	25°C		$\pm 4$		mV
Input Offset Current	$I_{IO}$		25°C		0.8		nA
			0°C~70°C		1.6		nA
Input Bias Current	$I_{IB}$		25°C		$\pm 1.8$		nA
			0°C~70°C		$\pm 2.2$		nA
Common-Mode Input Voltage Range	$V_{ICR}$		25°C	$\pm 13$	$\pm 14$		V
			0°C~70°C	$\pm 13$	$\pm 13.5$		V
Peak Output Voltage	$V_{OM}$	$R_L \geq 10k\Omega$	25°C	$\pm 12$	$\pm 13$		V
		$R_L \geq 2k\Omega$		$\pm 11.5$	$\pm 12.8$		V
		$R_L \geq 1k\Omega$	0°C~70°C		$\pm 12$		V
		$R_L \geq 2k\Omega$		$\pm 11$	$\pm 12.6$		V
Large-Signal Differential Voltage Amplification	$A_{VD}$	$V_{CC}=15V, V_O=1.4V \sim 11.4V, R_L \geq 500k\Omega$	25°C	100	400		V/mV
		$V_O = \pm 10, R_L = 2k\Omega$	25°C	120	400		V/mV
			0°C~70°C	100	400		V/mV
Unity-Gain Bandwidth	$B_1$		25°C	0.4	0.6		MHz
Input Resistance	$r_i$		25°C	8	33		M $\Omega$
Common-Mode Rejection Ratio	CMRR	$V_{IC} = \pm 13V, R_S = 50\Omega$	25°C	100	120		dB
			0°C~70°C	97	120		dB
Supply-Voltage Sensitivity ( $\Delta V_{IO}/\Delta V_{CC}$ )	SVRR	$V_{CC} = \pm 3V \sim \pm 18V, R_S = 50\Omega$	25°C		7	32	$\mu V/V$
			0°C~70°C		10	51	$\mu V/V$
Supply Current	$I_{CC}$	$V_O=0, \text{No load}$	25°C		2.67	5	mA

Notes: 1. Because long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a warranty. It is an engineering estimate of the averaged trend line of drift versus time over extended periods after the first 30 days of operation.

2. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

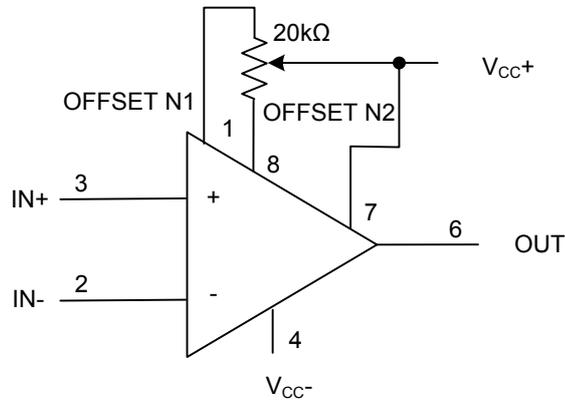
## ■ OPERATING CHARACTERISTICS

at specified free-air temperature,  $V_{CC}=5V$  (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS (Note 1)	MIN	TYP	MAX	UNIT
Input Offset Voltage	$V_n$	f=10Hz		10.5		$nV/\sqrt{Hz}$
		f=100Hz		10.2		
		f=1kHz		9.8		
Peak-to-Peak Equivalent Input Noise Voltage	$V_{N(PP)}$	f=0.1Hz~10Hz		0.38		$\mu V$
Equivalent Input Noise Current	$I_n$	f=10Hz		0.35		$nV/\sqrt{Hz}$
		f=100Hz		0.15		
		f=1kHz		0.13		
Peak-to-Peak Equivalent Input Noise Current	$I_{N(PP)}$	f=0.1Hz~10Hz		15		pA
Slew Rate	SR	$R_L \geq 2k\Omega$		0.3		V/ $\mu s$

Note: All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise noted.

■ APPLICATION CIRCUIT



Input Offset-Voltage Null Circuit

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