UNISONIC TECHNOLOGIES CO., LTD

CA3080

Preliminary

LINEAR INTEGRATED CIRCUIT

2MHz, OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

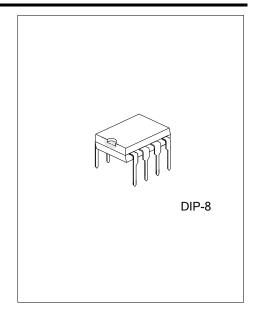
■ DESCRIPTION

The UTC **CA3080**, a high-performance operational -transconductance-amplifier (OTA) with Gatable-Gain Blocks, can be suitable applied in much several different conditions.

The UTC **CA3080**'s characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplexing, etc.

The UTC **CA3080** type has differential input and a single-ended, push-pull, class A output. In addition, this type has an amplifier bias input which may be used either for gating or for linear gain control. This type also has a high output impedance and it's transconductance (g_M) is directly proportional to the amplifier bias current (I_{ABC}) .

The UTC **CA3080** type is notable for its excellent slew rate $(50V/\mu s)$, which makes it especially useful for multiplexer and fast unity-gain voltage followers. This type is especially applicable for multiplexer applications because power is consumed only when the devices are in the "ON" channel state.

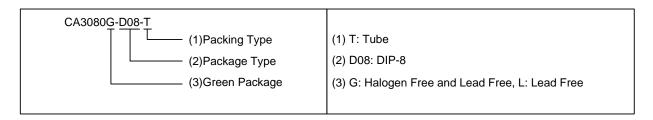


■ FEATURES

- * Slew Rate (Unity Gain, Compensated): 50V/µs
- * Adjustable Power Consumption: 10µW~30µW
- * Flexible Supply Voltage Range: ±2V~ ±15V
- * Fully Adjustable Gain: 0 to g_MR_L Limit

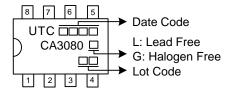
■ ORDERING INFORMATION

| Ordering | Package | Packing | |
|---------------|------------------------|---------|------|
| Lead Free | Lead Free Halogen Free | | |
| CA3080L-D08-T | CA3080G-D08-T | DIP-8 | Tube |

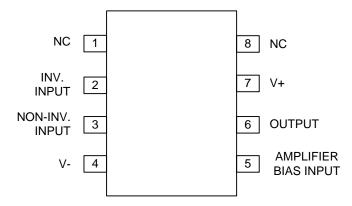


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■ MARKING



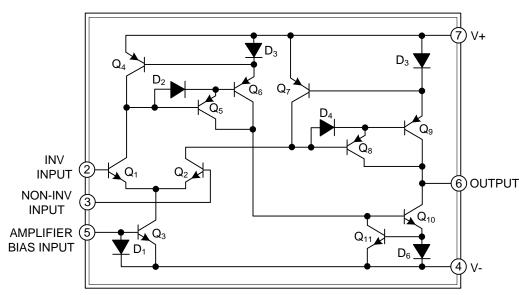
■ PIN CONFIGURATION



■ PIN DESCRIPTION

| PIN NO. | PIN NAME | DESCRIPTION |
|---------|----------------------|-------------------------|
| 1, 8 | NC | NC |
| 2 | INV- INPUT | Negative input |
| 3 | NON-INV INPUT | Positive input |
| 4 | V- | Negative supply voltage |
| 5 | AMPLIFIER BIAS INPUT | Bias input |
| 6 | OUTPUT | output |
| 7 | V+ | Positive supply voltage |
| 8 | NC | NC |

■ BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

| PARAMETER | SYMBOL | RATINGS | UNIT |
|--|------------------|------------|------|
| Supply Voltage (Between V+ and V- Terminal) | V _{CC} | 36 | V |
| Differential Input Voltage | V_{DI} | 5 | V |
| Input Voltage | V_{IN} | V+ ~ V- | |
| Input Signal Current | I _{SC} | 1 | mA |
| Amplifier Bias Current | I _{ABC} | 2 | mA |
| Maximum Junction Temperature (Plastic Package) | TJ | +150 | °C |
| Maximum Storage Temperature Range | T _{STG} | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|-------------------|------------------|------------|------|
| Temperature Range | T _{STG} | -40 ~ +125 | ů |

■ THERMAL DATA

| PARAMETER | SYMBOL | RATINGS | UNIT |
|------------------------------|---------------|---------|------|
| Thermal Resistance (Typical) | θ_{JA} | 130 | °C/W |

Note: θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

■ ELECTRICAL CHARACTERISTICS

For Equipment Design, $V_{\text{SUPPLY}} = \pm 15V$, Unless Otherwise Specified

| Tor Equipment Design, VSUP | PLY10V, | 0111000 011101 | moo opoomou | | | | |
|----------------------------------|-------------------|----------------------------------|--|------|-------|-------|------|
| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| Input Offset Voltage | | V | I _{ABC} =5µA | | 0.3 | 2 | mV |
| | | Vos | I _{ABC} =500μA | | 0.4 | 2 | mV |
| Input Offset Voltage Change |) | ΔV_{OS} | I _{ABC} =500μΑ~5μΑ | | 0.1 | | mV |
| put Offset Voltage Positive | | $\Delta V_{IO/V+}$ | I -500A | | | 150 | μV/V |
| Sensitivity | Negative | $\Delta V_{IO/V}$ | I _{ABC} =500μA | | | 150 | μV/V |
| Input Offset Current | | | 0.6 | μΑ | | | |
| Input Bias Current | | I_{B} | I _{ABC} =500μA | | 2 | 5 | μΑ |
| Differential Input Current | | I _{DI} | I _{ABC} =0, V _{DIFF} =4V | | 0.008 | 5 | nA |
| Amplifier Bias Voltage | | V_{BIAS} | I _{ABC} =500μA | | 0.71 | | V |
| Input Resistance | | R_{l} | I _{ABC} =500μA | | 36 | | kΩ |
| Input Capacitance | | Cı | I_{ABC} =500 μ A, f = 1MHz | | 5 | | pF |
| Input-to-Output Capacitance | • | C _I to C _O | I_{ABC} =500 μ A, f = 1MHz | | 0.024 | | pF |
| Common-Mode Input-Voltage | | V | - F00.1A | 12~ | 13.6~ | | V |
| Range | | V_{ic} | I _{ABC} =500μA | -12 | -14.5 | | V |
| Forward Transconductance | | am | I _{ABC} =500μA | 6700 | 9600 | 13000 | µmho |
| (Large Signal) | | gm | | 6700 | 9000 | 13000 | μππο |
| Output Capacitance | | Co | I_{ABC} =500 μ A, f = 1MHz | | 10 | | pF |
| Output Resistance | Output Resistance | | I _{ABC} =500μA | | 15 | | ΜΩ |
| Peak Output Current | | 1- | $I_{ABC}=5\mu A, R_L=0\Omega$ | 3 | 5 | 7 | μA |
| reak Output Current | | lo | I_{ABC} =500 μ A, R_L =0 Ω | 350 | 500 | 650 | μΑ |
| | Positive | V _{Om} | I _{ABC} =5μA, R _L =∞ | | 13.8 | | V |
| Peak Output Voltage | Negative | | IABC=5µA, KL-= | | -14.5 | | V |
| Feak Output Voltage | Positive | | L | 12 | 13.5 | | V |
| | Negative | | I _{ABC} =500μA, R _L =∞ | -12 | -14.4 | | V |
| Amplifier Supply Current | | Icc | I _{ABC} =500μA | 0.8 | 1.1 | 1.3 | mΑ |
| Device Dissipation | | P_D | I _{ABC} =500μA | 24 | 30 | 36 | mW |
| Magnitude of Leakage Current | | I _{IEAK} | I _{ABC} =0, V _{TP} =0 | | 0.08 | 5 | nA |
| | | | I _{ABC} =0, V _{TP} =36V | | 0.3 | 5 | nA |
| Propagation Delay T _P | | T _P | I _{ABC} =500μA | | 55 | | ns |
| Common-Mode Rejection Ratio CMRR | | CMRR | I _{ABC} =500μA | 80 | 110 | | dB |
| Open-Loop Bandwidth | | BW | I _{ABC} =500μA | | 2 | | MHz |
| Slew Rate | | CD | Uncompensated | | 75 | | V/µs |
| | | SR | Compensated | | 50 | | V/µs |
| - | | | | | | | |

■ TYPICAL APPLICATION CIRCUIT

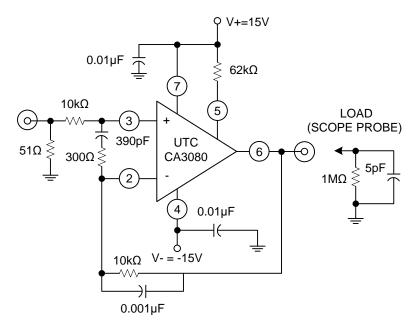
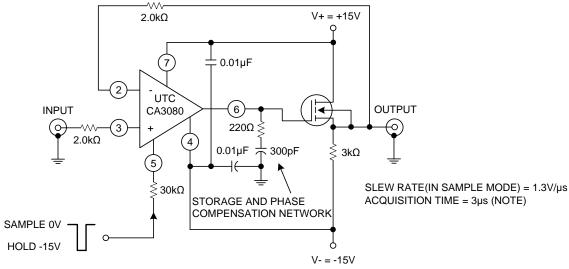


Figure 1. Schematic diaghram of the UTC CA3080 in a unity-gain voltage follower configuration



Note: Time required for output to settle within $\pm 3mV$ of a 4V step.

Figure 2. Schematic diagram of the UTC CA3080 in a sample-hold configuration

■ TYPICAL APPLICATION CIRCUIT (Cont.)

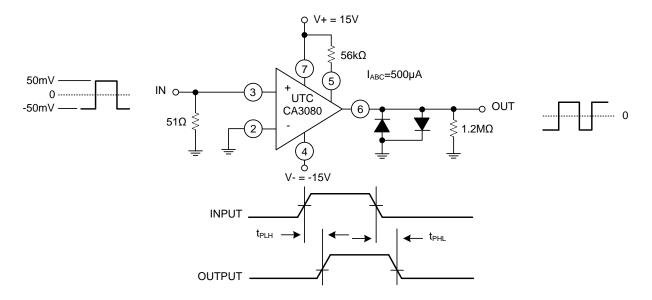


Figure 3. Propagation delay test circuit and associated waveforms

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