



U74AHCT158

Advance

CMOS IC

QUADRUPLE 2-LINE TO 1-LINE DATA SELECTORS/ MULTIPLEXERS

DESCRIPTION

The **U74AHCT158** is quadruple 2-line to 1-line data selectors/multiplexers are designed for 4.5V to 5.5V V_{CC} operation.

The **U74AHCT158** devices feature a common strobe (G) input. When the strobe is high, all outputs are high. When the strobe is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The devices provide inverted data.

FEATURES

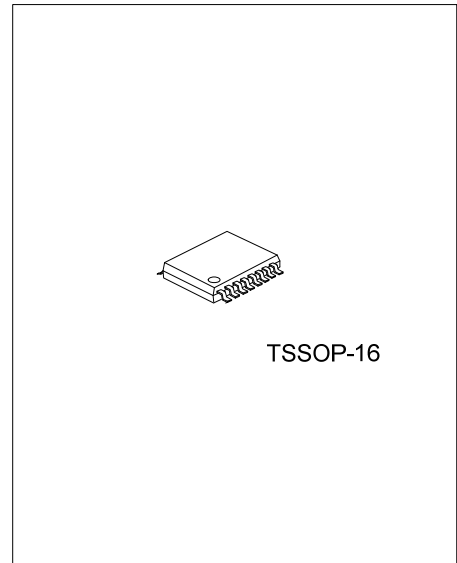
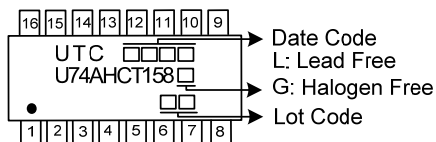
- * Input are TTL-Voltage Compatible
- * Low Quiescent Current: $I_{CC} = 2\mu A$ (Max.) at 5.5V
- * $\pm 8mA$ (Max.) output driver at 5V

ORDERING INFORMATION

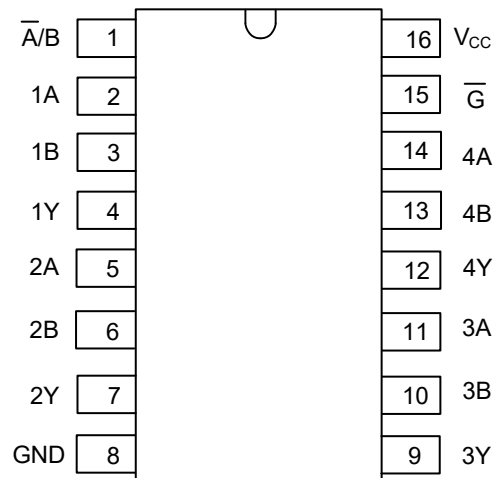
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AHCT158L-P16-R	U74AHCT158G-P16-R	TSSOP-16	Tape Reel

U74AHCT158G-P16-R	(1) Packing Type (2) Package Type (3) Green Package	(1) R: Tape Reel (2) P16: TSSOP-16 (3) G: Halogen Free and Lead Free, L: Lead Free
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MARKING



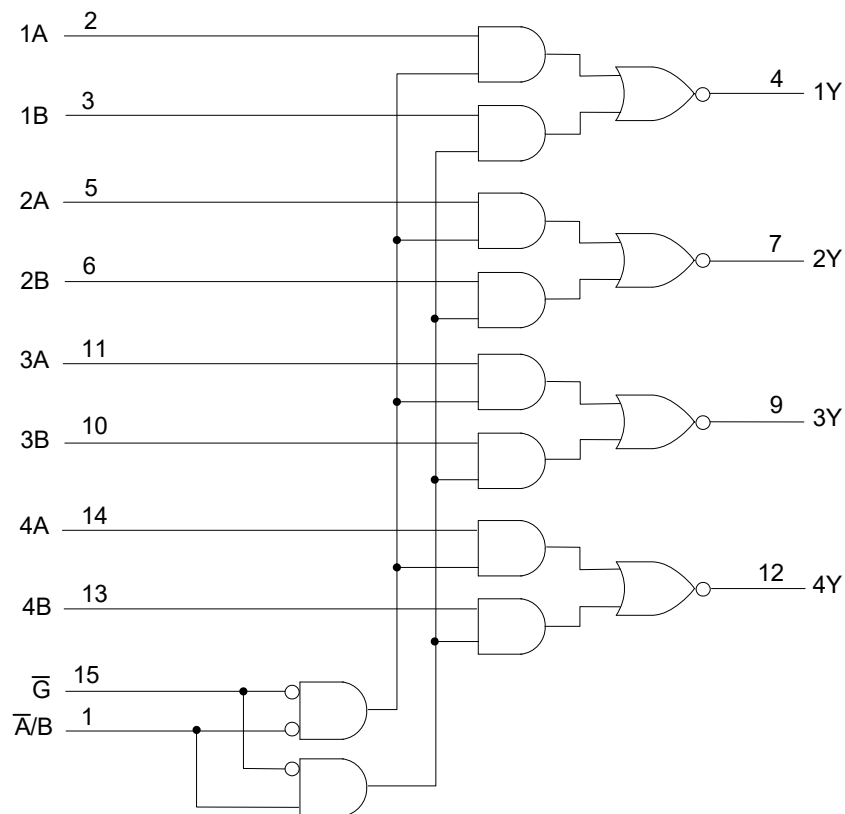
■ PIN CONFIGURATION



■ FUNCTION TABLE

INPUTS				OUTPUTS
\overline{G}	$\overline{A/B}$	A	B	Y
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

■ LOGIC DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5 ~ 7	V
Input Voltage	V_{IN}	-0.5 ~ 7	V
Output Voltage	V_{OUT}	-0.5 ~ $V_{CC}+0.5$	V
Continuous V_{CC} or GND Current	I_{CC}	±50	mA
Continuous Output Current	I_{OUT}	±25	mA
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	4.5 ~ 5.5	V
High-Level Input Voltage	V_{IH}	2	V
Low-Level Input Voltage	V_{IL}	0.8	V
Input Voltage	V_{IN}	0 ~ 5.5	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
High-Level Output Current	I_{OH}	-8	mA
Low-Level Output Current	I_{OL}	8	mA
Input Rise or Fall Times	$\Delta t/\Delta V$	20	ns/V
Operating Temperature	T_A	-40 ~ +125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Voltage High-Level	V_{OH}	$V_{CC}=4.5V, I_{OH}=-50\mu A$	4.4	4.5		V
		$V_{CC}=4.5V, I_{OH}=-8mA$	3.94			V
Output Voltage Low-Level	V_{OL}	$V_{CC}=4.5V, I_{OL}=50\mu A$			0.1	V
		$V_{CC}=4.5V, I_{OL}=8mA$			0.36	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0V \sim 5.5V, V_{IN}=5.5V$ or GND			±0.1	μA
Quiescent Supply Current	I_{CC}	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			2	μA
Additional quiescent supply current	ΔI_{CC} (Note)	$V_{CC}=5.5V$, one input at 3.4V, Other inputs at V_{CC} or GND			1.35	mA
Input Capacitance	C_I	$V_{CC}=5V, V_{IN}=V_{CC}$ or GND		2	10	pF

Note: This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0V or V_{CC} .

■ SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm0.5V$, unless otherwise specified)

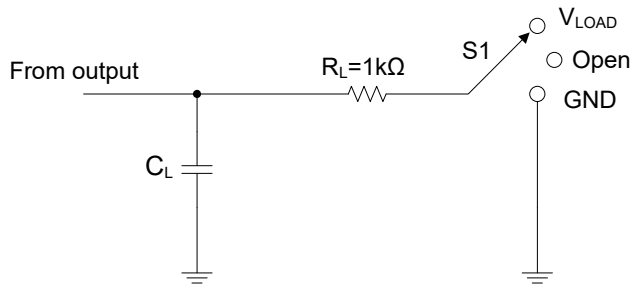
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay from input A or B to output Y	t_{PLH}	$C_L=15pF$		4.1	6.4	ns
		$C_L=50pF$		5.6	8.7	ns
	t_{PHL}	$C_L=15pF$		4.1	6.4	ns
		$C_L=50pF$		5.6	8.7	ns
Propagation delay from input \bar{A}/\bar{B} to output Y	t_{PLH}	$C_L=15pF$		5.3	8.1	ns
		$C_L=50pF$		6.8	10.4	ns
	t_{PHL}	$C_L=15pF$		5.3	8.1	ns
		$C_L=50pF$		6.8	10.4	ns
Propagation delay from input \bar{G} to output Y	t_{PLH}	$C_L=15pF$		5.6	8.6	ns
		$C_L=50pF$		7.1	11	ns
	t_{PHL}	$C_L=15pF$		5.6	8.6	ns
		$C_L=50pF$		7.1	11	ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation capacitance	C_{PD}	$V_{CC}=5V$, $f=1MHz$, No load		11		pF

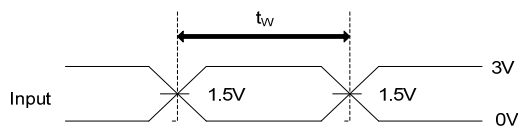
Note: Characteristics are for surface-mount packages only.

■ TEST CIRCUIT AND WAVEFORMS

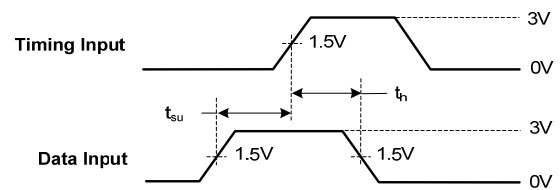


Test Circuit

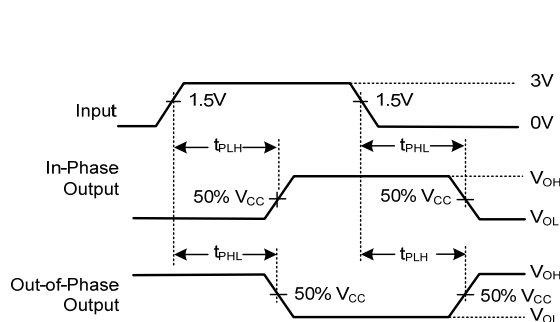
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



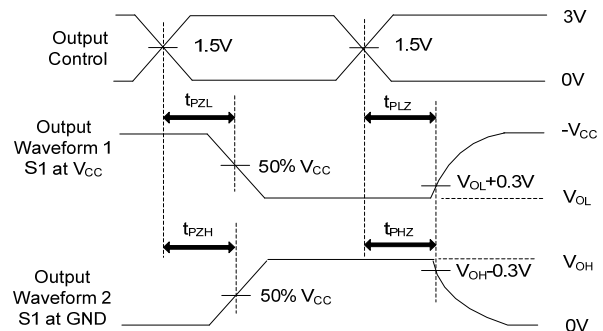
PULSE DURATION



SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Notes: 1. C_L includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics: $P_{RR} \leq 1\text{MHz}$, $Z_O = 50\Omega$, $t_r \leq 3\text{ns}$, $t_f \leq 3\text{ns}$.

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