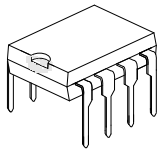
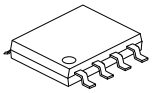
4.5MHz, OPERATION AMPLIFIER WITH MOSFET INPUT/BIPOLAR OUTPUT



DIP-8



SOP-8

■ DESCRIPTION

The UTC **CA3140** is integrated circuit operational amplifier that combine the advantages of high voltage PMOS transistors with high voltage bipolar transistors on a single monolithic chip.

The UTC **CA3140** operational amplifier feature gate protected MOSFET (PMOS) transistors in the input circuit to provide very high input impedance, very low input current, and high speed performance. The UTC **CA3140** operates at supply voltage from 4V to 36V (either single or dual supply). This is internally phase compensated to achieve stable operation in unity gain follower operation, and additionally, has access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS field effect transistors in the input stage results in common mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute for single supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load terminal short circuiting to either supply rail or to ground.

The UTC **CA3140** is intended for operation at supply voltages up to 36V (±18V).

■ FEATURES

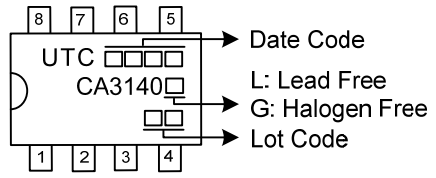
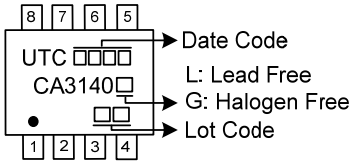
* MOSFET Input Stage
  - Very High Input Impedance (Z_{IN}) -1.5TΩ (Typ)
  - Very Low Input Current ($I_{I)}$ -10pA (Typ) at ±15V
  - Wide Common Mode Input Voltage Range (V_{ICR}) - Can be SWUNG 0.5V Below Negative Supply Voltage Rail

■ ORDERING INFORMATION

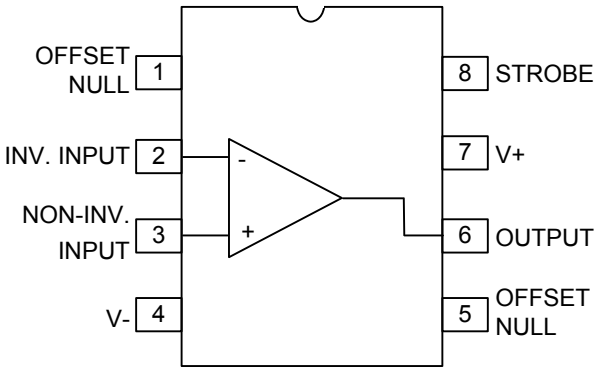
Ordering Number		Package	Packing
Lead Free	Halogen Free		
CA3140L-D08-T	CA3140G-D08-T	DIP-8	Tube
CA3140L-S08-R	CA3140G-S08-R	SOP-8	Tape Reel

CA3140G-D08-T (1)Packing Type (2)Package Type (3)Green Package	(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

DIP-8	SOP-8
	

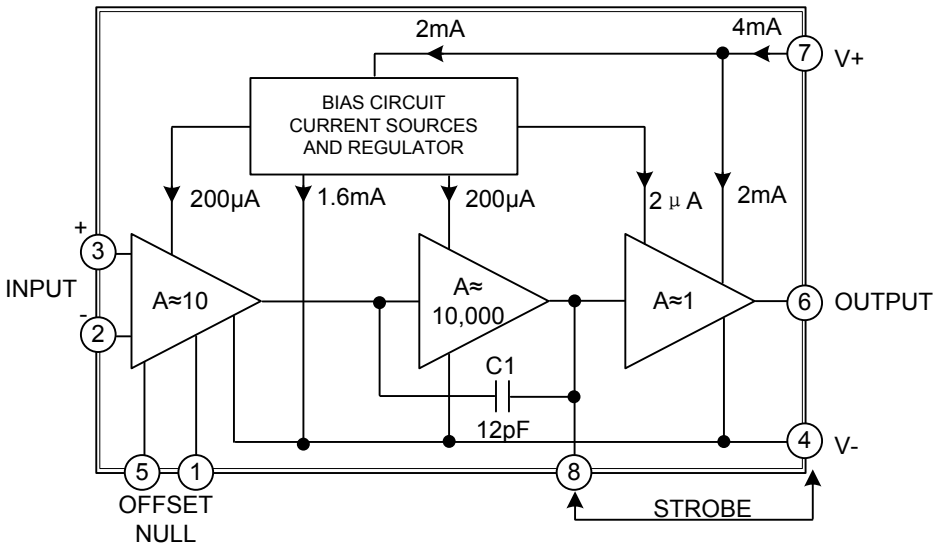
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	OFFSET NULL	Offset null
2	INV. INPUT	Inverting input
3	NON-INV. INPUT	Non-inverting input
4	V-	Negative power supply
5	OFFSET NULL	Offset null
6	OUTPUT	Output
7	V+	Positive power supply
8	STROBE	A supplementary phase compensated terminal

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Between V+ and V- Terminals)	V^{+}_{MAX}	36	V
Differential Mode Input Voltage	V_{DM}	8	V
DC Input Voltage	V_{IN}	(V+ +8V) ~ (V- -0.5V)	V
Input Terminal Current	I_{IN}	1	mA
Output Short Circuit Duration∞ (Note 2)		Indefinite	
Maximum Junction Temperature (Plastic Package)	T_J	+150	°C
Operating Conditions Temperature Range	T_{OTR}	-40 ~ +125	°C
Maximum Storage Temperature Range	T_{STG}	-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Short circuit may be applied to ground or to either supply.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient	DIP-8	θ_{JA}	115	°C/W
	SOP-8		165	°C/W

■ ELECTRICAL CHARACTERISTICS

(V_{SUPPLY} = ±15V, T_A = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Offset Voltage Adjustment Resistor		Typical Value of Resistor Between Terminals 4 and 5 or 4 and 1 to Adjust Max V_{IO}			4.7		kΩ
Input Resistance	R_I				1.5		TΩ
Input Capacitance	C_I				4		pF
Output Resistance	R_O				60		Ω
Equivalent Wideband Input Noise Voltage	e_N	BW=140kHz, R_S=1MΩ			48		μV
Equivalent Input Noise Voltage	e_N	R_S=100Ω, f=1kHz			40		nV/$\sqrt{Hz}$
		R_S=100Ω, f=10kHz			12		nV/$\sqrt{Hz}$
Short Circuit Current to Opposite Supply	I_{OM}+	Source			33		mA
	I_{OM}-	Sink			20		mA
Gain-Bandwidth Product	f_T				4.5		MHz
Slew Rate	SR				2		V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low					220		μA
Transient Response	t_r	R_L= 2kΩ, C_L= 100pF	Rise Time		0.08		μs
	O_S		Overshoot		10		%
Settling Time at 10VP-P	t_S	R_L= 2kΩ, C_L= 100pF Voltage Follower	To 1mV		4.5		μs
			To 10mV		1.4		μs

■ ELECTRICAL CHARACTERISTICS

(For Equipment Design, at V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$\|V_{IO}\|$			5	15	mV
Input Offset Current	$\|I_{IO}\|$			0.5	30	pA
Input Current	I_I			10	50	pA
Large Signal Voltage Gain (Note 3)	A_{OL}		86	95		dB
Common Mode Rejection Ratio	CMRR		70	85		dB
Common Mode Input Voltage Range	V_{ICR}		-15		12	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_S$	PSRR		76	100		dB
Max Output Voltage (Note 4)	V_{OM}+	R_L=2kΩ	+12	13		V
	V_{OM}-	R_L=2kΩ	-14	-14.4		V
Supply Current	I+			4	6	mA
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta_T$			8		μV/°C

Notes: 1. At V_O = 26V_{P-P}, +12V, -14V and R_L = 2kΩ.
2. At R_L = 2kΩ.

■ ELECTRICAL CHARACTERISTICS

(For Design Guidance, at V+ = 5V, V- = 0V, T_A = 25°C, Unless Otherwise Specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$\|V_{IO}\|$			5		mV
Input Offset Current	$\|I_{IO}\|$			0.1		pA
Input Current	I_I			2		pA
Input Resistance	R_I			1		TΩ
Large Signal Voltage Gain	A_{OL}			95		dB
Common Mode Rejection Ratio	CMRR			85		dB
Common Mode Input Voltage Range	V_{ICR}			0		V
				2.6		V
Power Supply Rejection Ratio	PSRR ΔVIO/ΔVS			80		dB
Maximum Output Current	V_{OM}+	R_L=2kΩ		3		V
	V_{OM}-	R_L=2kΩ		0.13		V
Maximum Output Current	I_{OM}+	Source		10		mA
	I_{OM}-	Sink		1		mA
Slew Rate	SR			2		V/μs
Gain-Bandwidth Product	f_T			3.7		MHz
Supply Current (See Figure 32)	I+			0.8		mA
Sink Current from Terminal 8 to Terminal 4 to Swing Output Low				200		μA

■ TYPICAL APPLICATIONS

Offset Voltage Nulling

The input offset voltage can be nulled by connecting a 10kΩ potentiometer between Terminals 1 and 5 and returning its wiper arm to terminal 4, see Figure 1A. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotationis not fully utilized. Typical values of series resistors (R) that may be placed at either end of the potentiometer, see Figure 1B, to optimize its utilization range are given in the Electrical Specifications table. An alternate system is shown in Figure 1C. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to 0Ω at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

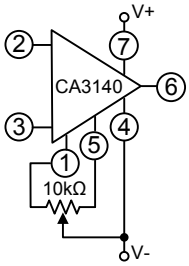


Figure 1A. BASIC

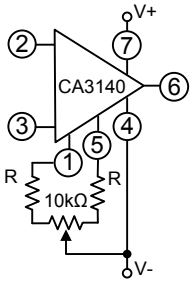


Figure 1B. IMPROVED RESOLUTION

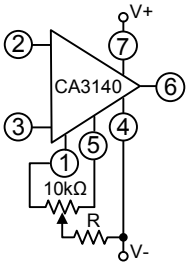


Figure 1C. SIMPLER IMPROVED RESOLUTION

Figure 1. THREE OFFSET VOLTAGE NULLING METHODS