LCD Driver for 280 Display Units BL55080

General Description

The BL55080 is a general LCD driver IC for 280 units LCD panel. It features a wide operating supply voltage range, incorporates simple communication interface with microcomputer and is suitable for multiple application.

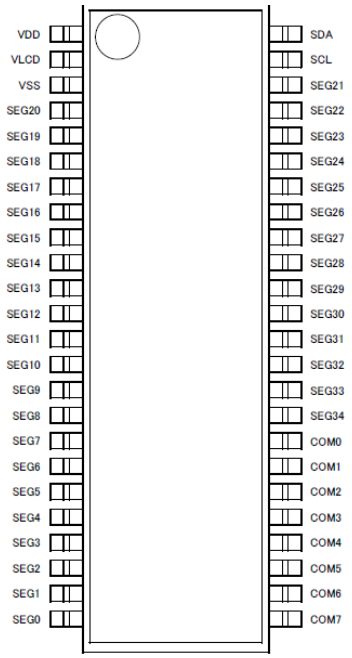
Features

- LCD drive output : 8 Common output, 35 Segment output
- Integrated RAM for display data: 35*8=280bit
- Serial data interface(I2C): SDA, SCL
- Integrated Oscillator circuit
- Integrated Buffer AMP for LCD driving, 1/4 Bias, 1/8 Duty
- No external components
- Low power consumption design
- Integrated EVR(Electrical volume register) function
- Supply Voltage Range: 2.5V~5.5V
- LCD drive power supply Range: 2.5V~5.5V
- Excellent EMC immunity
- Compatible with general microcomputer
- TSSOP48, LQFP48, LQFP52 package

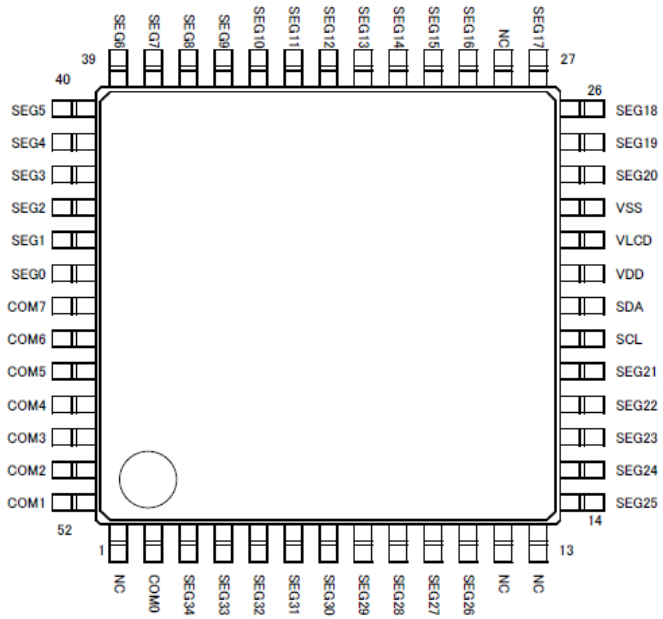
Application

Power Meter, Gas Meter…
FAX
Car audio
Portable equipment
Home electrical appliance
Toy, Clock
Industrial instrument
Etc.

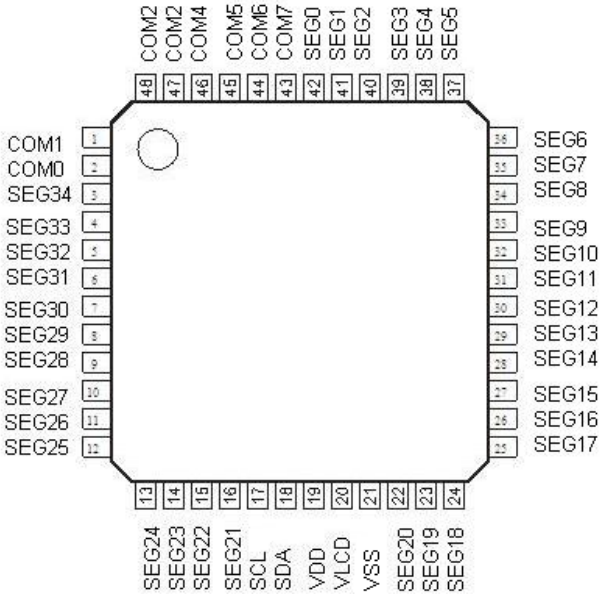
Pin Assignment



TSSOP48



LQFP52



LQFP48

Figure 1

Pin Description

Pin No			Symbol	Description
TSSOP48	LQFP52	LQFP48		
48	20	18	SDA	Serial data input
47	19	17	SCL	Serial transfer clock
1	21	19	Vdd	Power supply
2	22	20	Vlcd	Power supply for LCD drive
3	23	21	Vss	GND

4-24 33-46	3-11 14-18 24-27 29-52	3-16 22-42	SEG0-34	Segment output
25-32	2, 46-52	1-2 43-48	COM0-7	Common output
	1, 12, 13, 28		NC	Not connected

Table 1

Block Diagram

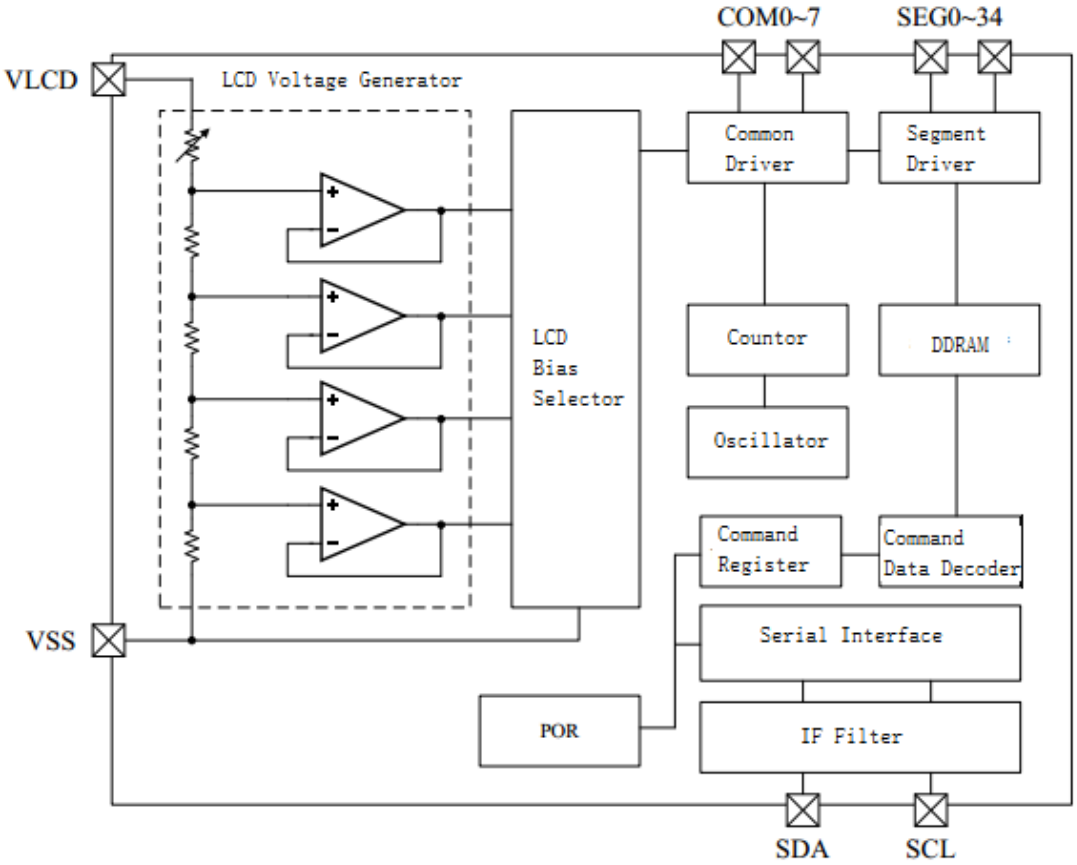


Figure 2

Function Description

Function Circuit

The BL55080 has all function circuits that can directly drive LCD containing up to 8 commons and up to 35 segments. The function circuits include:Power-on reset, LCD bias selector, LCD voltage generator, Oscillator, display RAM, Common/segment outputs, etc.

Display Function Decription

The display RAM is a static 35x 8-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment;

similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the common outputs.

BIT	0	1	2	3	4	5	6	7	·····	21h	22h	
0	a	i										COM0
1	b	j										COM1
2	c	k										COM2
3	d	l										COM3
4	e	m										COM4
5	f	n										COM5
6	g	o										COM6
7	h	p										COM7
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG33	SEG34	

Table 2

When display data is transmitted to the BL55080, the display bytes received are stored in the display RAM. To illustrate the filling order, an example of a 7-segment numeric display showing the drive mode is given; the RAM filling organization depicted applies equally to other LCD types.

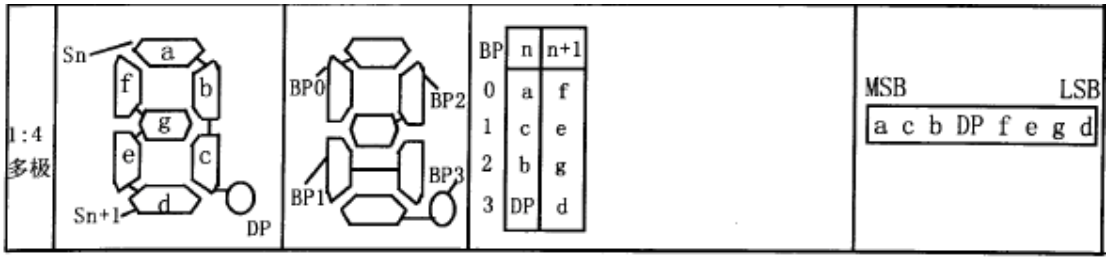


Figure 3

I²C-bus protocol

Two I2C-bus slave addresses (01111100) are reserved for the BL55080.

The I2C-bus protocol is shown in Fig.4. The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by BL55080 slave address. After acknowledgement, one or more command bytes (m) follow which define the status of the BL55080. The last command byte is tagged with a cleared most significant bit, the continuation bit C. After the last command byte, a series of display data bytes(n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the BL55080. The acknowledgement after each byte is made by the BL55080. After the last display byte, the I2C-bus master issues a STOP condition (P).

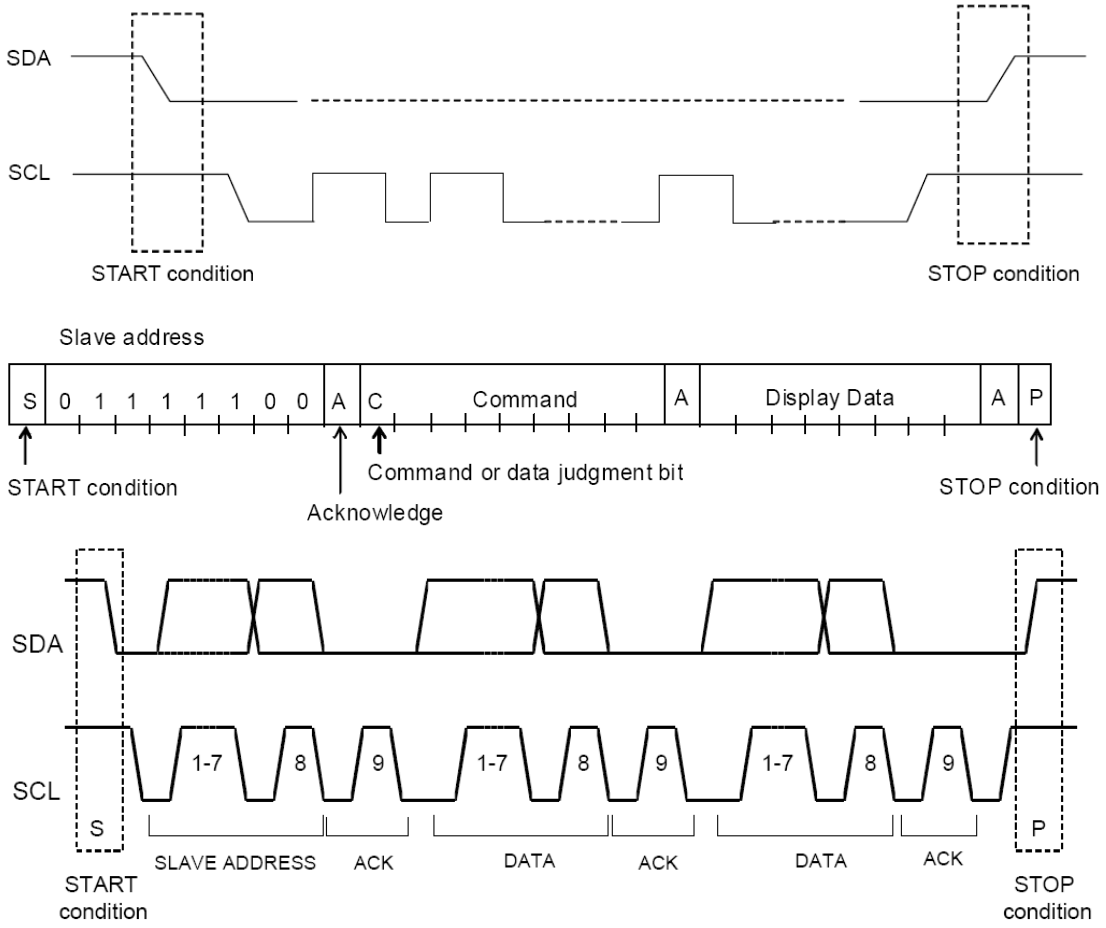


Figure 4

Command Decoder

The command decoder identifies command bytes that arrive on the I^{2}C-bus. All available commands carry a continuation bit C in their most significant bit position. The five commands available to the BL55080 are defined.

	Command	Function
1	Address set (ADSET)	DDRAM address setting (00h~22h)
2	EVR set (EVRSET)	EVR setting (0~31)
3	Display Control (DISCTL)	Frame Frequency, Power save mode setting
4	IC operation set (ICSET)	LCD drive mode, software reset, display on/off
5	All pixel Control (APCTL)	All pixel control during display ON

Table 3

ADSET

	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Value	C	0	Addr[5:0]					
default	C	0	0	0	0	0	0	0

Address set

The address range can be set as 00 to 22H for write mode.when the specified address is out of range, the address will be set to 00.

The address can be set 23H and 24H for read mode. The addresses(23H/24H) are Command register addresses.

EVRSET

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	0	EVR[4:0]				
default	C	1	0	0	0	0	0	0

This is used to control a 32-step electrical volume register (EVR). This register is used to set V0 voltage level (the max level voltage of LCD driving voltage)

The relationships of electrical volume register setting and V0 voltage:

○The relationship of electrical volume register (EVR) setting and V0 voltage

EVR	Calculation formula	VLCD= 5.500	VLCD= 5.000	VLCD= 4.000	VLCD= 3.500	VLCD= 3.000	VLCD= 2.500	[V]
0	VLCD	V0= 5.500	V0= 5.000	V0= 4.000	V0= 3.500	V0= 3.000	V0= 2.500	[V]
1	0.967*VLCD	V0= 5.323	V0= 4.839	V0= 3.871	V0= 3.387	V0= 2.903	V0= 2.419	[V]
2	0.937*VLCD	V0= 5.156	V0= 4.688	V0= 3.750	V0= 3.281	V0= 2.813	V0= 2.344	[V]
3	0.909*VLCD	V0= 5.000	V0= 4.545	V0= 3.636	V0= 3.182	V0= 2.727	V0= 2.273	[V]
4	0.882*VLCD	V0= 4.853	V0= 4.412	V0= 3.529	V0= 3.088	V0= 2.647	V0= 2.206	[V]
5	0.857*VLCD	V0= 4.714	V0= 4.286	V0= 3.429	V0= 3.000	V0= 2.571	V0= 2.143	[V]
6	0.833*VLCD	V0= 4.583	V0= 4.167	V0= 3.333	V0= 2.917	V0= 2.500	V0= 2.083	[V]
7	0.810*VLCD	V0= 4.459	V0= 4.054	V0= 3.243	V0= 2.838	V0= 2.432	V0= 2.027	[V]
8	0.789*VLCD	V0= 4.342	V0= 3.947	V0= 3.158	V0= 2.763	V0= 2.368	V0= 1.974	[V]
9	0.769*VLCD	V0= 4.231	V0= 3.846	V0= 3.077	V0= 2.692	V0= 2.308	V0= 1.923	[V]
10	0.750*VLCD	V0= 4.125	V0= 3.750	V0= 3.000	V0= 2.625	V0= 2.250	V0= 1.875	[V]
11	0.731*VLCD	V0= 4.024	V0= 3.659	V0= 2.927	V0= 2.561	V0= 2.195	V0= 1.829	[V]
12	0.714*VLCD	V0= 3.929	V0= 3.571	V0= 2.857	V0= 2.500	V0= 2.143	V0= 1.786	[V]
13	0.697*VLCD	V0= 3.837	V0= 3.488	V0= 2.791	V0= 2.442	V0= 2.093	V0= 1.744	[V]
14	0.681*VLCD	V0= 3.750	V0= 3.409	V0= 2.727	V0= 2.386	V0= 2.045	V0= 1.705	[V]
15	0.666*VLCD	V0= 3.667	V0= 3.333	V0= 2.667	V0= 2.333	V0= 2.000	V0= 1.667	[V]
16	0.652*VLCD	V0= 3.587	V0= 3.261	V0= 2.609	V0= 2.283	V0= 1.957	V0= 1.630	[V]
17	0.638*VLCD	V0= 3.511	V0= 3.191	V0= 2.553	V0= 2.234	V0= 1.915	V0= 1.596	[V]
18	0.625*VLCD	V0= 3.438	V0= 3.125	V0= 2.500	V0= 2.188	V0= 1.875	V0= 1.563	[V]
19	0.612*VLCD	V0= 3.367	V0= 3.061	V0= 2.449	V0= 2.143	V0= 1.837	V0= 1.531	[V]
20	0.600*VLCD	V0= 3.300	V0= 3.000	V0= 2.400	V0= 2.100	V0= 1.800	V0= 1.500	[V]
21	0.588*VLCD	V0= 3.235	V0= 2.941	V0= 2.353	V0= 2.059	V0= 1.765	V0= 1.471	[V]
22	0.576*VLCD	V0= 3.173	V0= 2.885	V0= 2.308	V0= 2.019	V0= 1.731	V0= 1.442	[V]
23	0.566*VLCD	V0= 3.113	V0= 2.830	V0= 2.264	V0= 1.981	V0= 1.698	V0= 1.415	[V]
24	0.555*VLCD	V0= 3.056	V0= 2.778	V0= 2.222	V0= 1.944	V0= 1.667	V0= 1.389	[V]
25	0.545*VLCD	V0= 3.000	V0= 2.727	V0= 2.182	V0= 1.909	V0= 1.636	V0= 1.364	[V]
26	0.535*VLCD	V0= 2.946	V0= 2.679	V0= 2.143	V0= 1.875	V0= 1.607	V0= 1.339	[V]
27	0.526*VLCD	V0= 2.895	V0= 2.632	V0= 2.105	V0= 1.842	V0= 1.579	V0= 1.316	[V]
28	0.517*VLCD	V0= 2.845	V0= 2.586	V0= 2.069	V0= 1.810	V0= 1.552	V0= 1.293	[V]
29	0.508*VLCD	V0= 2.797	V0= 2.542	V0= 2.034	V0= 1.780	V0= 1.525	V0= 1.271	[V]
30	0.500*VLCD	V0= 2.750	V0= 2.500	V0= 2.000	V0= 1.750	V0= 1.500	V0= 1.250	[V]
31	0.491*VLCD	V0= 2.705	V0= 2.459	V0= 1.967	V0= 1.721	V0= 1.475	V0= 1.230	[V]

Prohibited setting

*In case EVR is used, please satisfy VLCD-V0 >0.6 V condition.
If this condition cannot be satisfied, IC output will be unstable.
*Do not use V0 < 2.5V area. If EVR is set to this area, IC operation will be unstable.

Table 4

DISCTL

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	0	Fr[1:0]		Sr[1:0]	
default	C	1	1	0	0	0	1	0

Display control

[3:2]: frame frequency control (FR)

00 - 80Hz (default)

01 - 69.565Hz

10 - 64Hz

11 - 50Hz

[1:0]: power save mode control (SR)

00 – power save mode 1

01 – power save mode 2

10 – normal mode (default)

11 – hight power mode

ICSET

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	1	0	Mode	softrst	dison
default	C	1	1	1	0	1	0	0

Set IC

[2]：LCD drive mode

0 - line inversion mode

1 - frame inversion mode; (default)

[1]：software reset

0 – no operation (default)

1 – software reset

[0]：display on/off control

0 – display off (default)

1 – display on

APCTL

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	1	1	0	Apon	Apoff
Default	C	1	1	1	1	0	0	0

All pixel control, this register is effective only at “DISPLAY ON” status.

[1]：all pixel ON control

0 – normal (default)

1 – all pixel on

[0]：all pixel OFF control

0 – normal (default)

1 – all pixel off

When Apon and Apoff=1, Apoff is selected. Apoff has higher priority than Apon.

Initialize sequence example

No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0→5[V] (Tr=0.1[ms])
	↓									
2	wait 100us									Initialize IC
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
5	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
6	ICSET	1	1	1	1	0	*	1	*	Software Reset
	↓									
7	DISCTL	1	1	1	0	0	0	1	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
8	EVRSET	1	1	0	0	0	0	0	0	Unnecessary when initial value setup
	↓									(If you need to change the condition)
9	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
10	Display Data	*	*	*	*	*	*	*	*	Address 00h
	⋮									⋮
	Display Data	*	*	*	*	*	*	*	*	Address 22h
	↓									
11	Stop									Stop condition
	↓									
12	Start									Start condition
13	Slave address	0	1	1	1	1	1	0	0	Issue slave address
	↓									
14	ICSET	1	1	1	1	0	*	0	1	Display ON

Table 5

Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Supply voltage	Vdd	-0.5～+6.0	V
LCD operating voltage	Vlcd	0～ Vdd	V
Input voltage	Vi	Vss-0.5～Vdd+0.5	V
Operating temperature	Topr	-40～ +85	℃
Storage temperature	Tstg	-65～ +150	℃

Electric Characteristic(Ta=25℃)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vdd	IC Operating voltage		2.5	-	5.5	V
Vlcd	LCD operating voltage		2.5	-	5.5	V
IST	Standby current	Display off, Oscillation off			0.5	μA
IDD	Power consumption	Vdd=3.3V,Vlcd=5V,Ta=25℃,power save mode1, FR=80Hz,1/4 bias,Frame inversion		2	5	μA
ILCD	LCD power consumption	Vdd=3.3V,Vlcd=5V,Ta=25℃,power save mode1, FR=80Hz,1/4 bias,Frame inversion		6	10	μA
FCLK	Frame frequency	Vdd=3.3V, FR=80Hz setting	60	80	110	Hz
V_{CM}	DC voltage component	C_{COM}=32nF, COM0~COM7	-20		20	mV
V_S		C_S=4.7nF, SEG0~SEG34	-20		20	mV

NOTE: the voltage of DC voltage component test: VDD=3.3 V , VLCD=5V, EVR=8, Ta=25℃

Typical Application

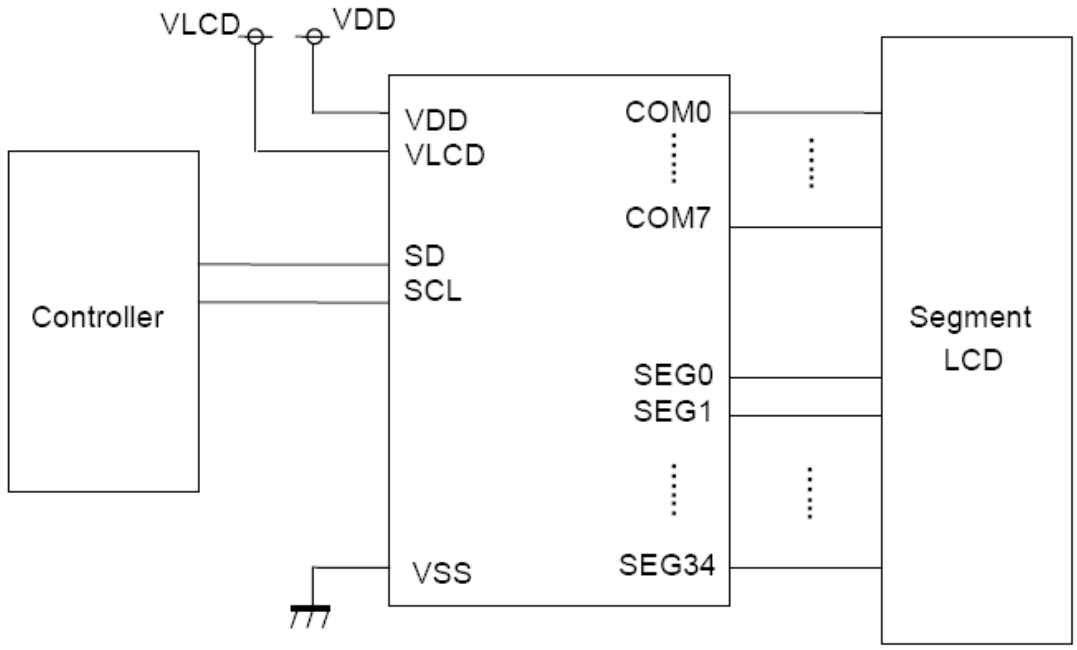


Figure 5

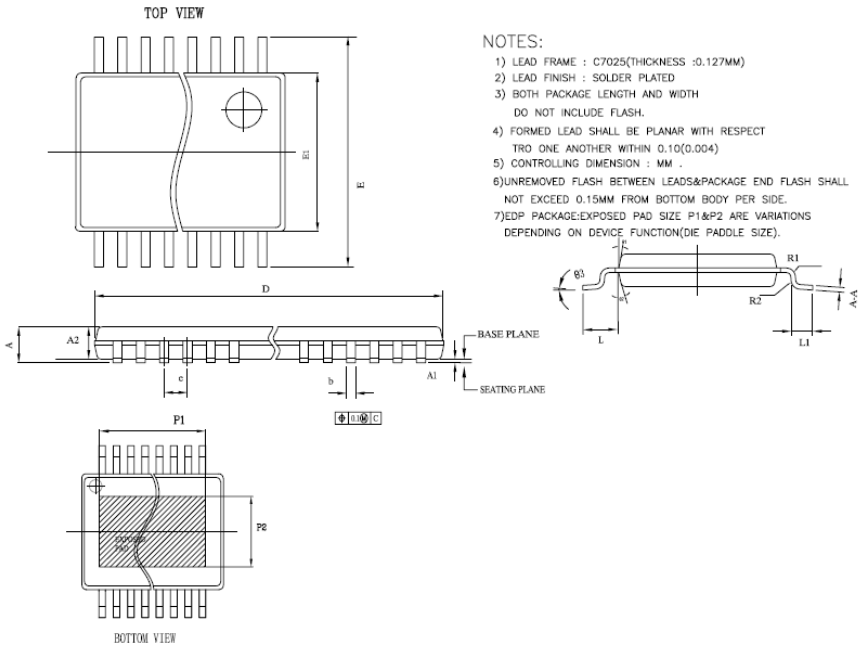
Application Note:

Please set power up condition in order to ensure POR operation.

1) The VDD and VLCD need be powered up simultaneously. Or power up VDD first, then power up VLCD. the rising time of Vdd must more than 1mS
2) The VDD and VLCD need be powered off simultaneously. Or power off VLCD first, then power off VLCD.

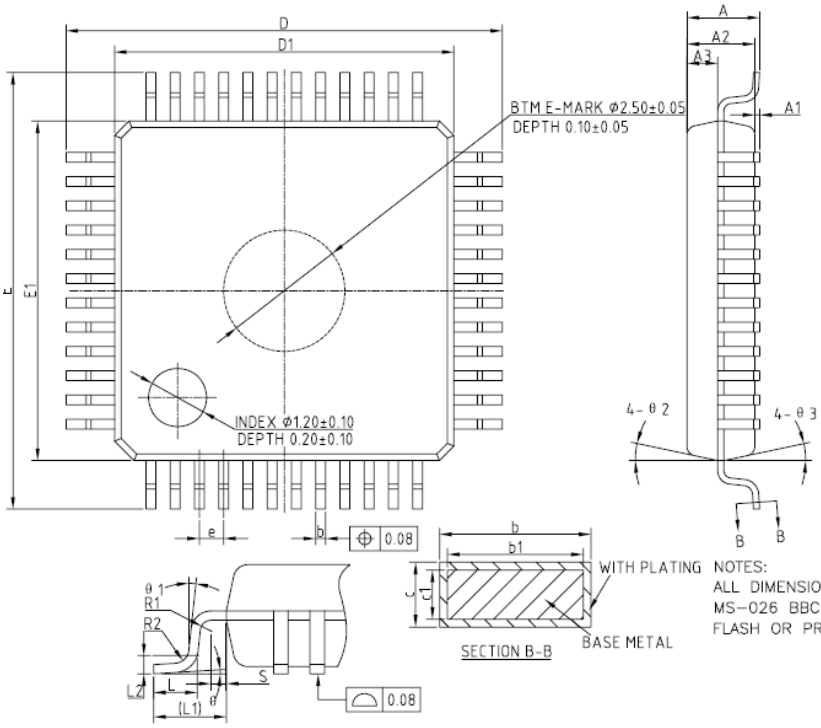
Package Outlines

TSSOP48



Symbol	TSSOP48	
	Min	Max
A		1.2
A1	0.03	0.13
A2	0.824	1.024
E	7.9	8.3
E1	6	6.2
D	12.4	12.6
L	0.35	0.65
L1	0.35	0.65
e	0.5	
b	0.17	0.27
R1	0.22TYP	
R2	0.22TYP	
A-A	0.12	0.22
θ1	12° TYP	
θ2	12° TYP	
θ3		

LQFP48

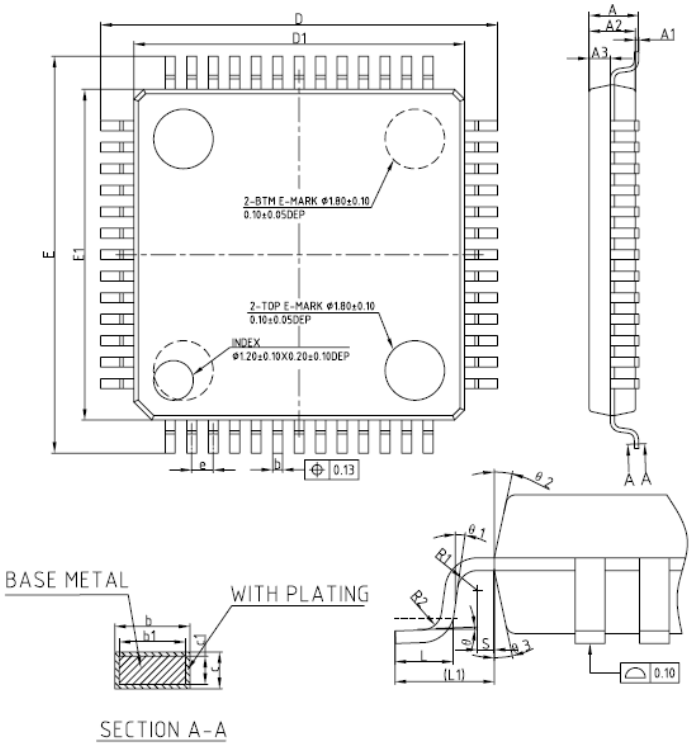


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.13	–	0.18
c1	0.12	0.127	0.134
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e		0.50BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	0.20
S	0.20	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BBC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

LQFP52



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.20
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.28	–	0.37
b1	0.27	0.30	0.33
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R1	0.08	–	–
R2	0.08	–	–
S	0.15	–	–
θ	0°	3.5°	7°
θ1	0°	–	–
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-026 BCE DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.