

NCE N-Channel Enhancement Mode Power MOSFET

Description

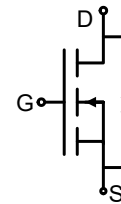
The NCE0102Y uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

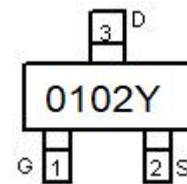
- $V_{DS} = 100V, I_D = 2A$
 $R_{DS(ON)} < 220m\Omega @ V_{GS}=10V$ (Typ:190m Ω)
 $R_{DS(ON)} < 240m\Omega @ V_{GS}=4.5V$ (Typ:200m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply



Schematic diagram



Marking and pin assignment



SOT-23-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
0102Y	NCE0102Y	SOT-23-3L	Ø180mm	8 mm	3000 units

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	2	A
Drain Current-Continuous($T_C=100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	1.4	A
Drain Current-Pulsed (Note 1)	I_{DM}	8	A
Maximum Power Dissipation	P_D	1.25	W
Avalanche Current (Note 1)	I_{AR}	2	A
Single pulse avalanche energy (Note 5)	E_{AS}	2.45	mJ
Reverse diode dv/dt, $V_{DS} \leq 80\text{ V}$, $I_{SD} < I_D$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

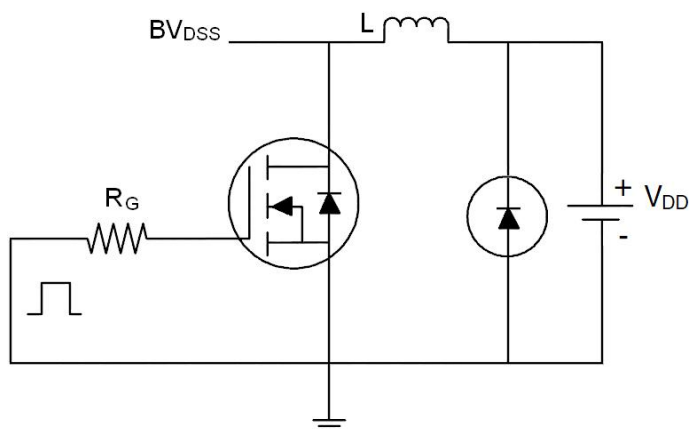
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =2A	-	190	220	mΩ
		V _{GS} =4.5V, I _D =2A	-	200	240	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =2A	1	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	360.6	-	PF
Output Capacitance	C _{oss}		-	24.6	-	PF
Reverse Transfer Capacitance	C _{rss}		-	13	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, R _L =25Ω V _{GS} =10V, R _G =1Ω	-	6	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	12	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =2A, V _{GS} =10V	-	12.0		nC
Gate-Source Charge	Q _{gs}		-	1.8	-	nC
Gate-Drain Charge	Q _{gd}		-	2.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =2A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	2	A

Notes:

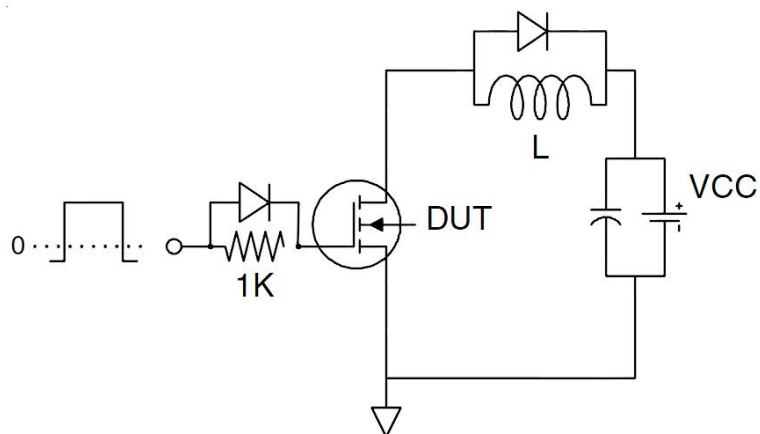
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test Circuit

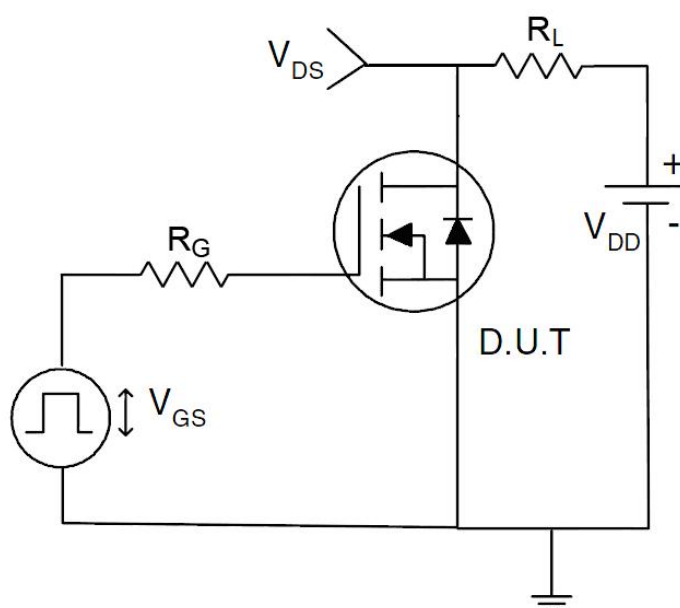
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

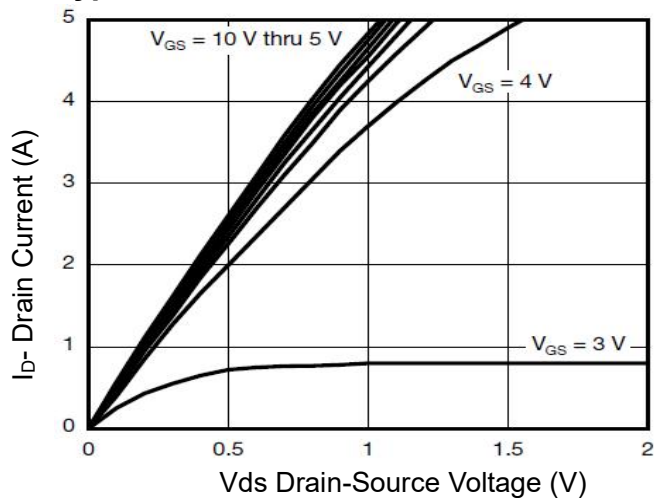


Figure 1 Output Characteristics

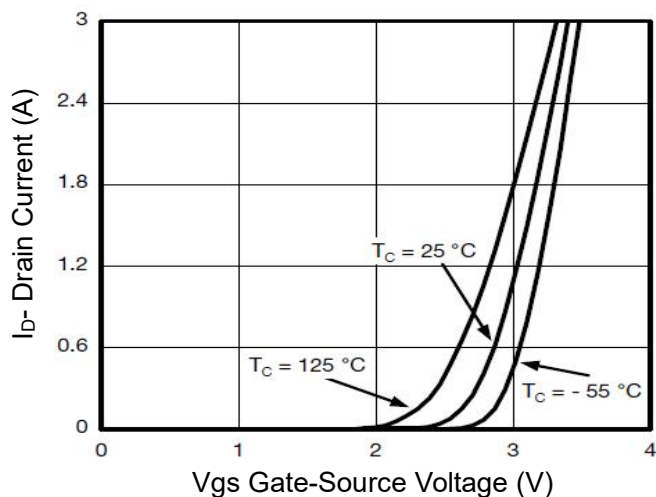


Figure 2 Transfer Characteristics

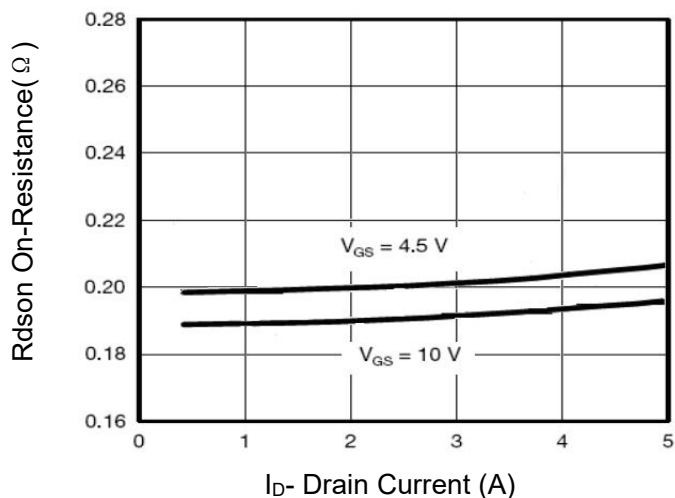


Figure 3 Rdson- Drain Current

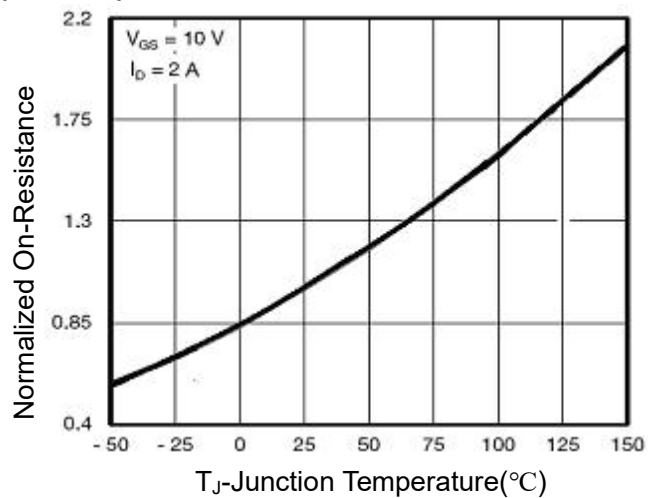


Figure 4 Rdson-Junction Temperature

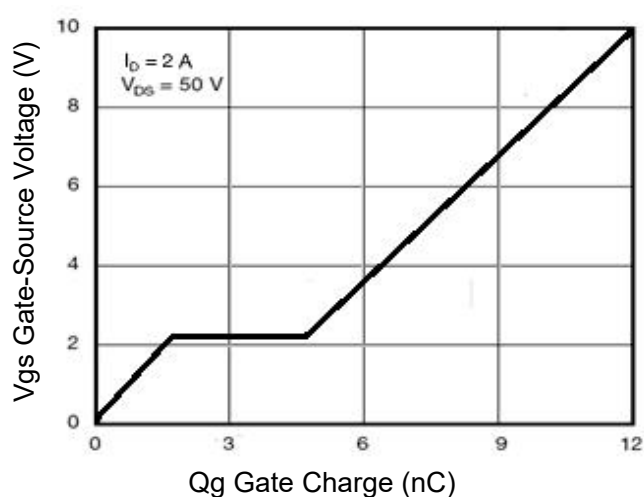


Figure 5 Gate Charge

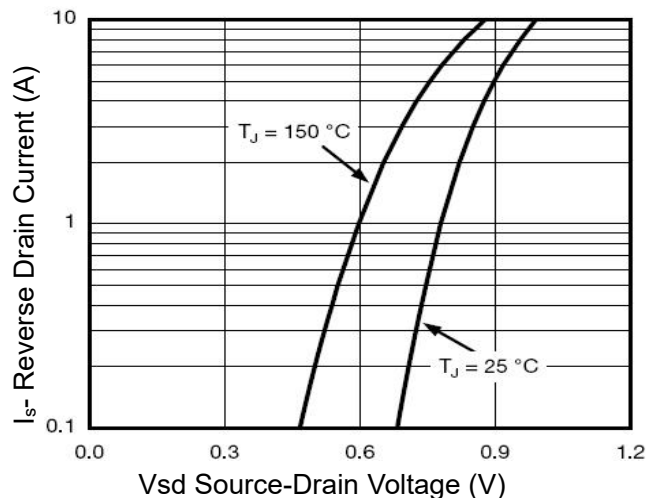


Figure 6 Source- Drain Diode Forward

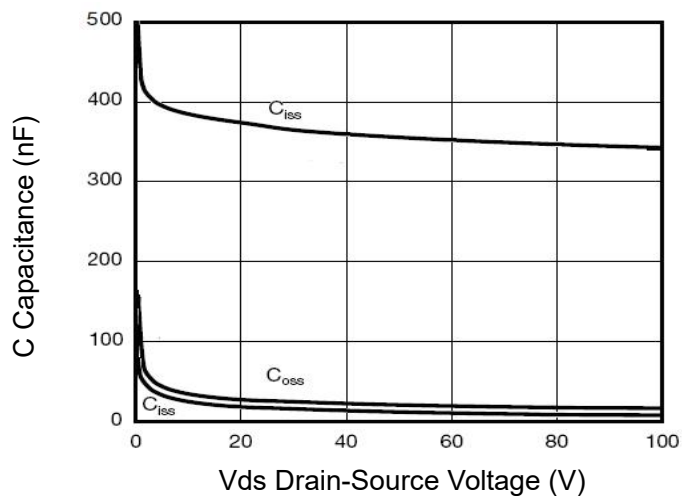


Figure 7 Capacitance vs Vds

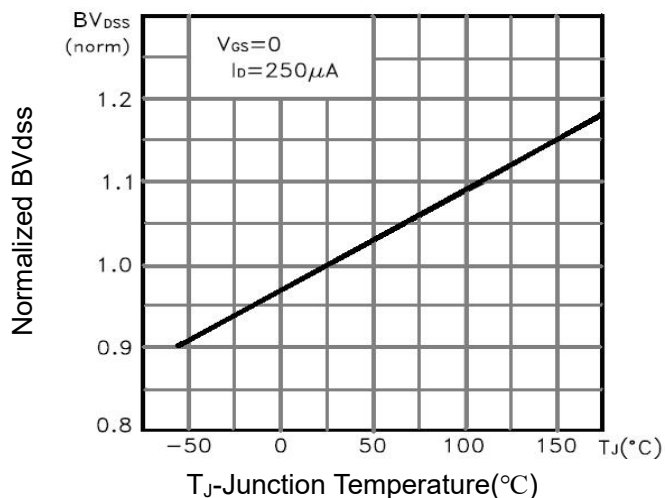


Figure 9 BV_{DSS} vs Junction Temperature

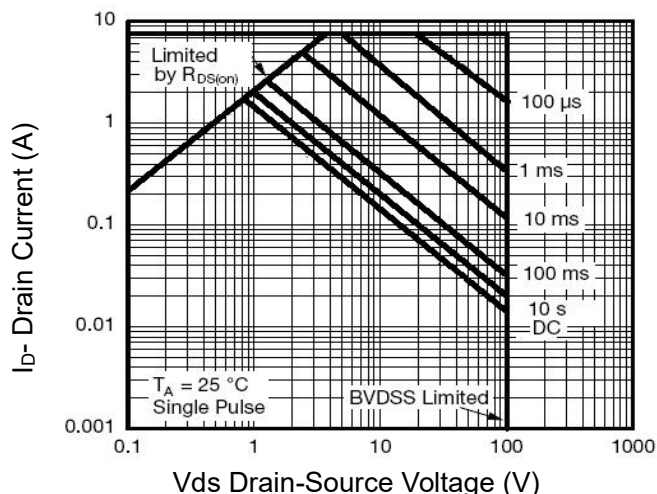


Figure 8 Safe Operation Area

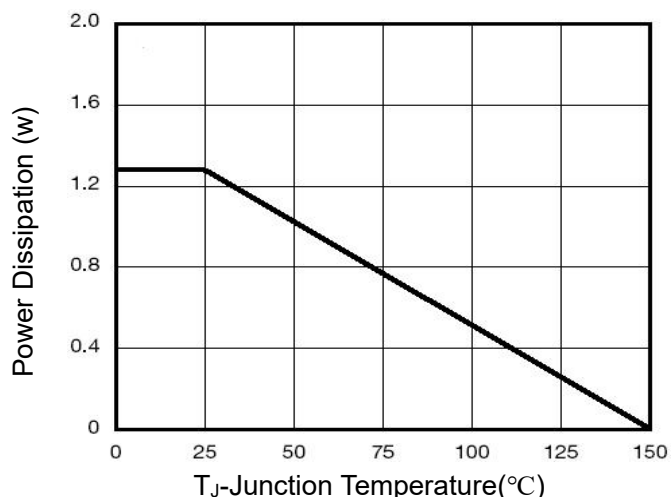


Figure 10 Power De-rati

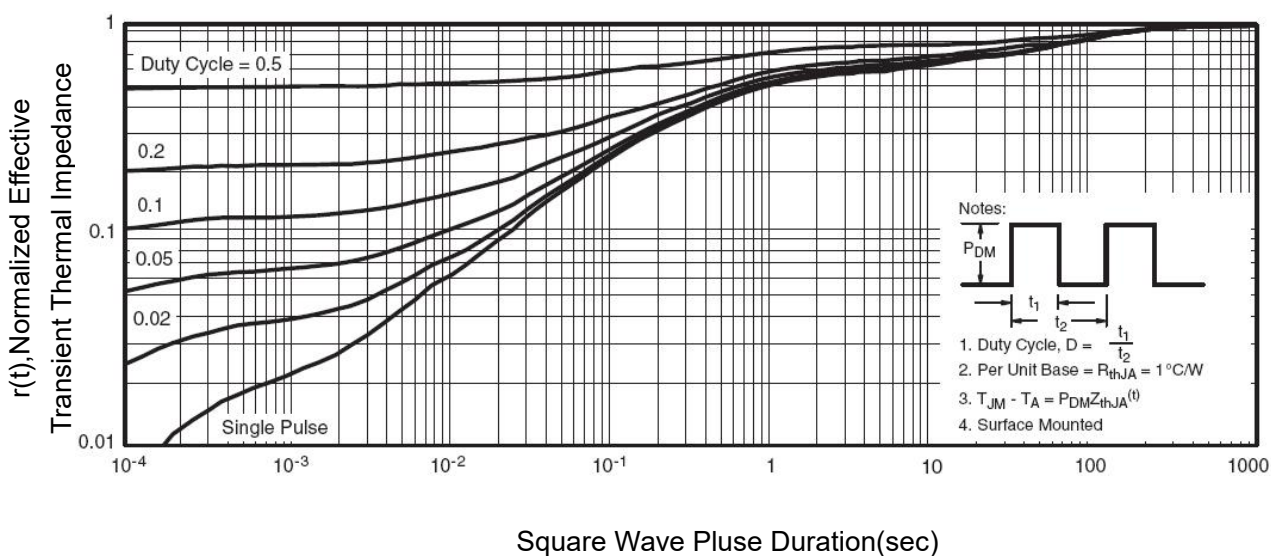
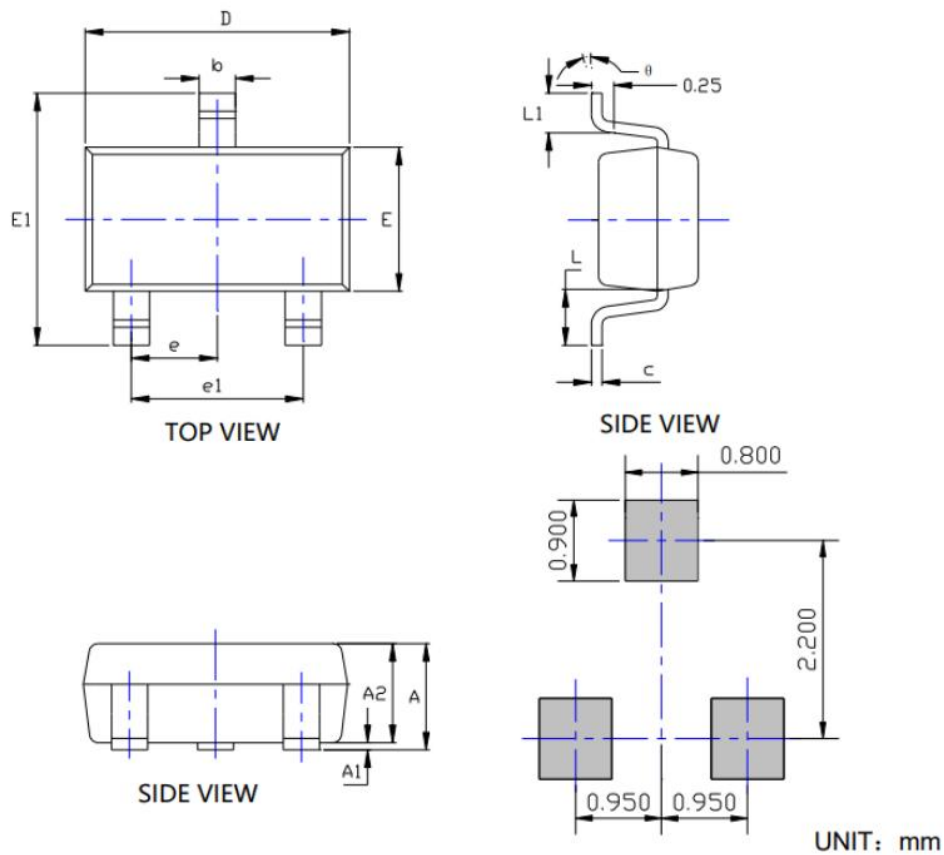


Figure 11 Normalized Maximum Transient Thermal Impedance

SOT-23-3L Package Information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.041	---	0.049	1.050	---	1.250
A1	0.000	---	0.008	0.000	---	0.200
A2	0.041	0.043	0.045	1.050	1.100	1.150
b	0.012	0.016	0.020	0.300	0.400	0.500
c	0.004	---	0.008	0.100	---	0.200
D	0.111	0.115	0.119	2.820	2.920	3.020
E	0.059	0.063	0.067	1.500	1.600	1.700
E1	0.104	0.110	0.116	2.650	2.800	2.950
e	0.037TYP			0.950TYP		
e1	0.071	0.075	0.079	1.800	1.900	2.000
L	0.024REF			0.600REF		
L1	0.012	0.018	0.024	0.300	0.450	0.600
θ	0°	---	8°	0°	---	8°

NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

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