

## NCE N-Channel Enhancement Mode Power MOSFET

### Description

The NCE0117AK uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

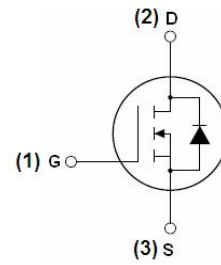
- $V_{DS} = 100V, I_D = 17A$   
 $R_{DS(ON)} < 48m\Omega @ V_{GS}=10V$  (Typ:42m $\Omega$ )  
 $R_{DS(ON)} < 53m\Omega @ V_{GS}=4.5V$  (Typ:44m $\Omega$ )
- High density cell design for ultra low  $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

### Application

- Power switching application
- Hard switched and high frequency circuits

**100% UIS TESTED!**

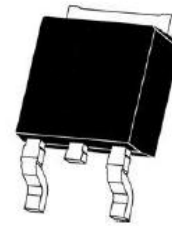
**100%  $\Delta V_{DS}$  TESTED!**



Schematic diagram



Marking and pin assignment



TO-252-2L top view

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE0117AK	NCE0117AK	TO-252-2L	-	-	-

### Absolute Maximum Ratings ( $T_C=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	17	A
Drain Current-Continuous( $T_C=100^\circ C$ )	$I_D(100^\circ C)$	12	A
Pulsed Drain Current	$I_{DM}$	60	A
Maximum Power Dissipation	$P_D$	55	W
Single pulse avalanche energy (Note 5)	$E_{AS}$	29	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.73	$^{\circ}\text{C/W}$
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## Electrical Characteristics ( $T_c=25^{\circ}\text{C}$ unless otherwise noted)

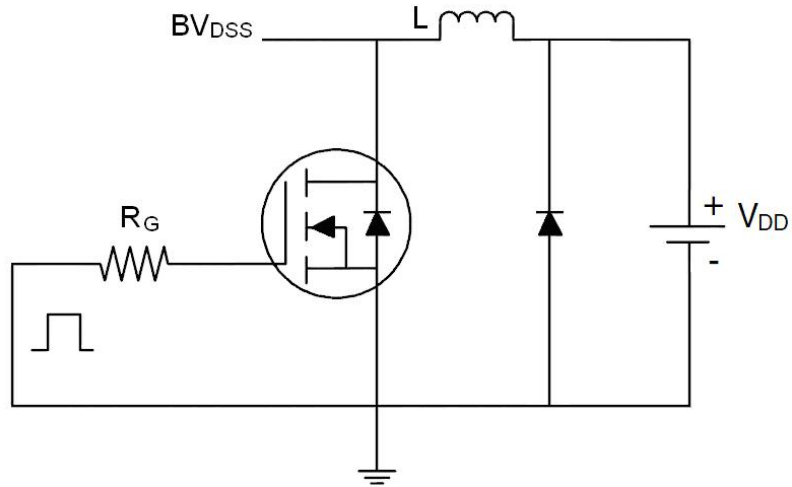
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	100	110	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =100V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.6	2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	-	42	48	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A		44	53	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =10A	-	14	-	S
Dynamic Characteristics <sup>(Note4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, F=1.0MHz	-	1468	-	PF
Output Capacitance	C <sub>oss</sub>		-	62	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	13.6	-	PF
Switching Characteristics <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =30V, R <sub>L</sub> =15Ω V <sub>GS</sub> =10V, R <sub>G</sub> =2.5Ω	-	13.8	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	9.3	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	43.8	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	11.4	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, I <sub>D</sub> =10A, V <sub>GS</sub> =10V	-	40	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	4.4	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	9.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =17A	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	17	A
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

## Notes:

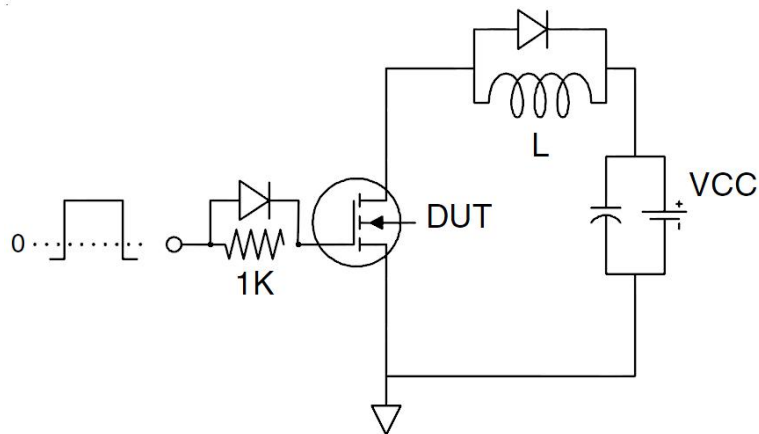
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_G=25\Omega$

## Test Circuit

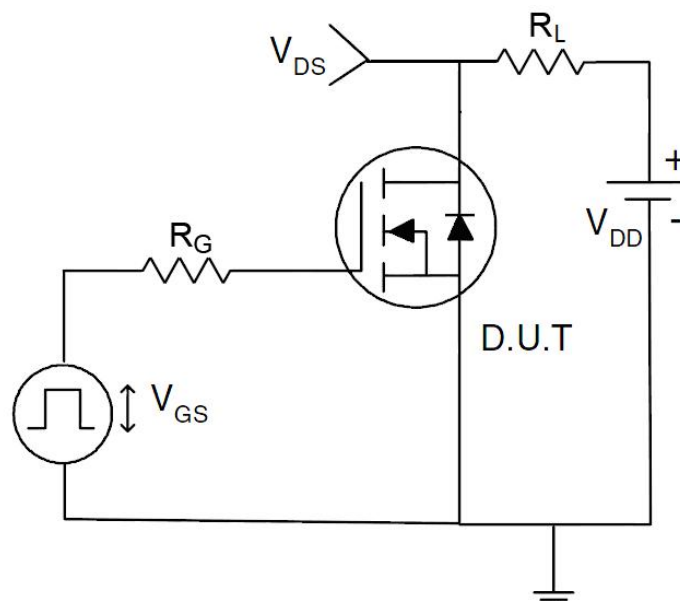
### 1) $E_{AS}$ test Circuit



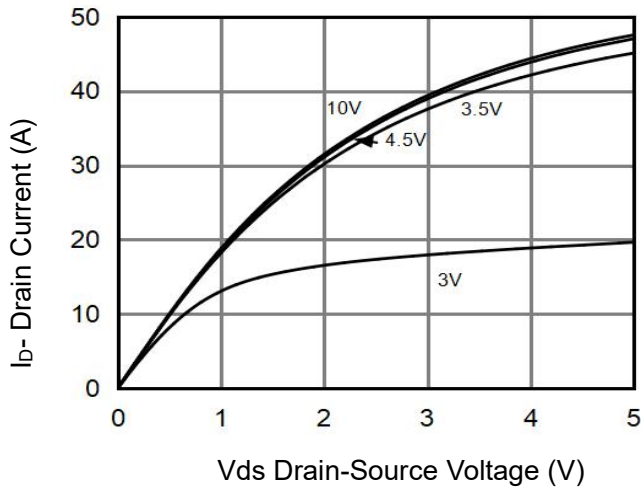
### 2) Gate charge test Circuit



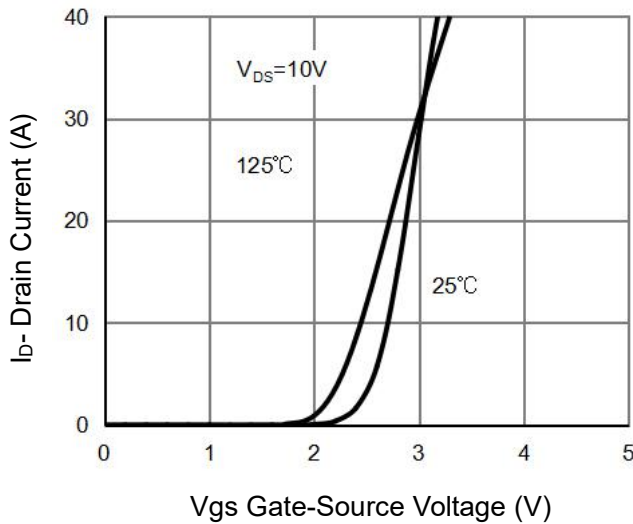
### 3) Switch Time Test Circuit



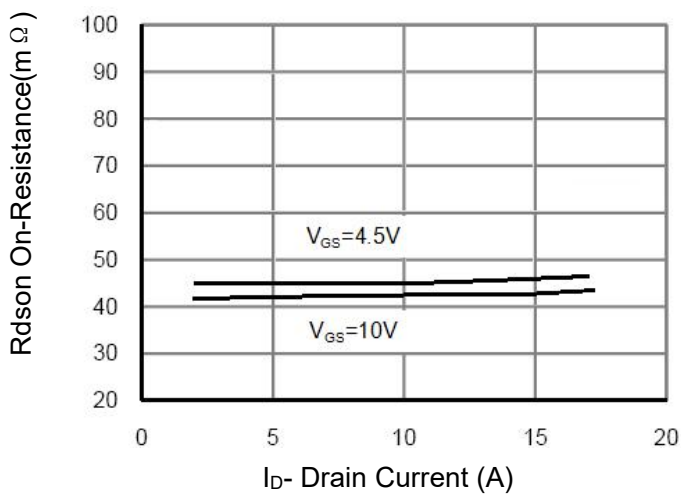
## Typical Electrical and Thermal Characteristics (Curves)



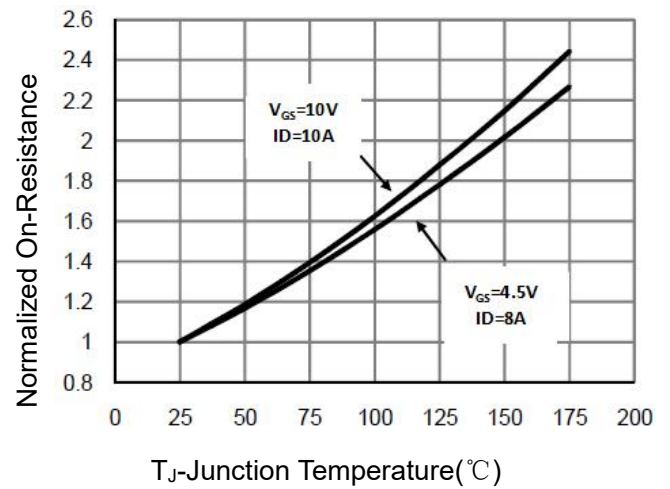
**Figure 1 Output Characteristics**



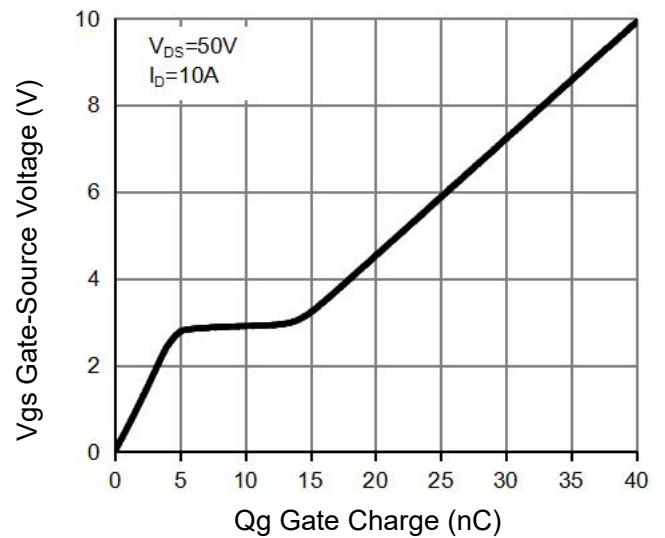
**Figure 2 Transfer Characteristics**



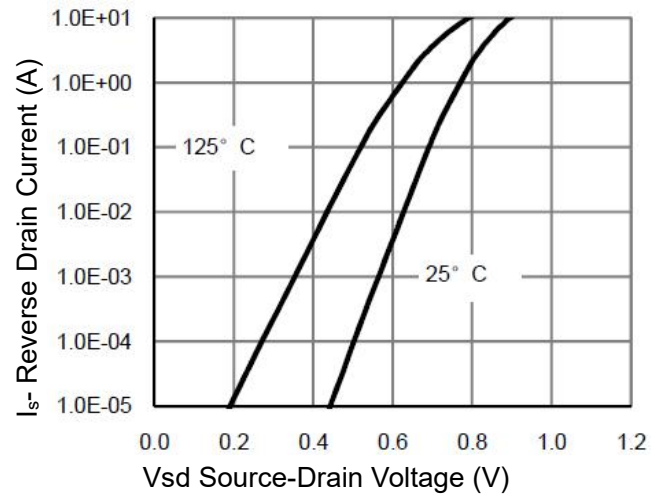
**Figure 3  $R_{DS(on)}$  - Drain Current**



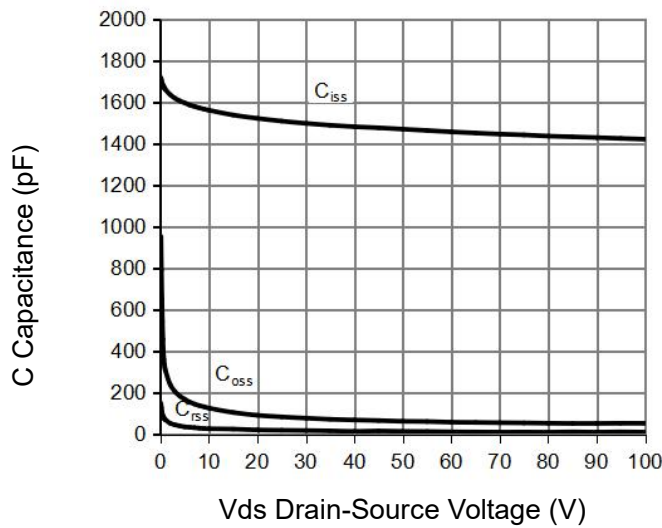
**Figure 4  $R_{DS(on)}$ -Junction Temperature**



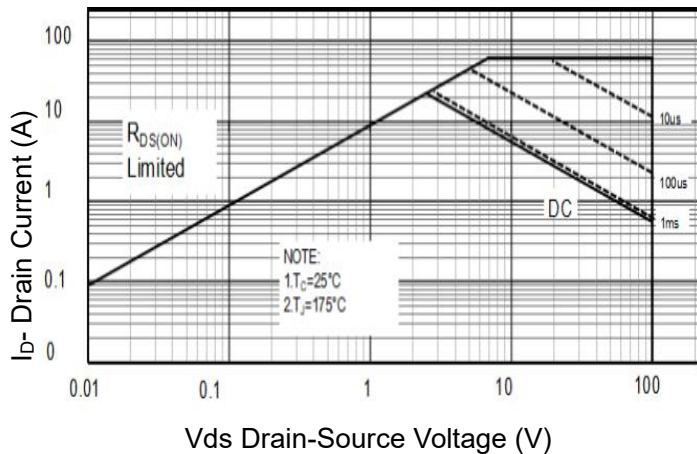
**Figure 5 Gate Charge**



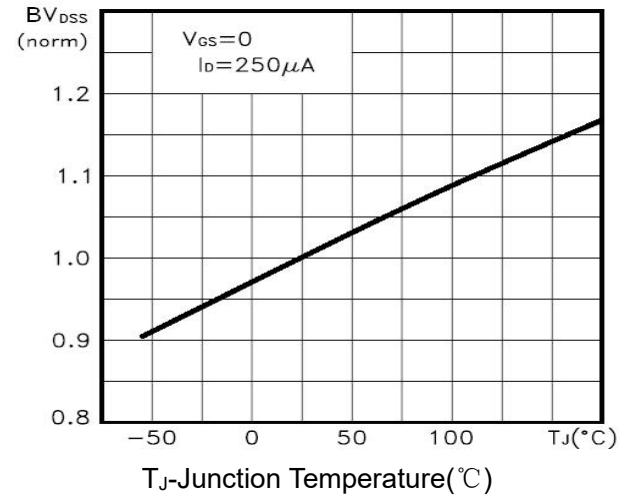
**Figure 6 Source- Drain Diode Forward**



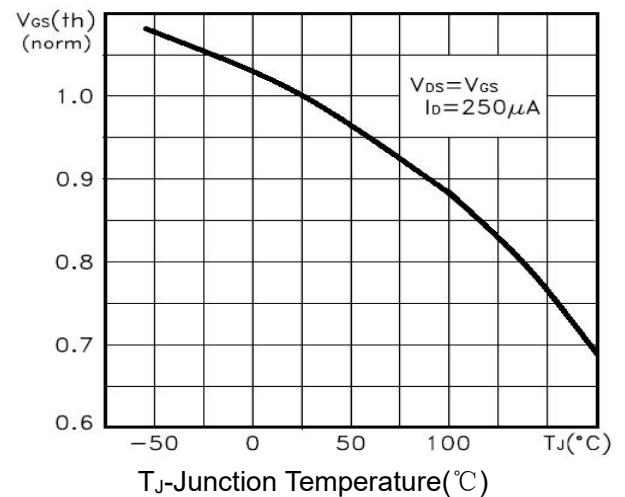
**Figure 7 Capacitance vs Vds**



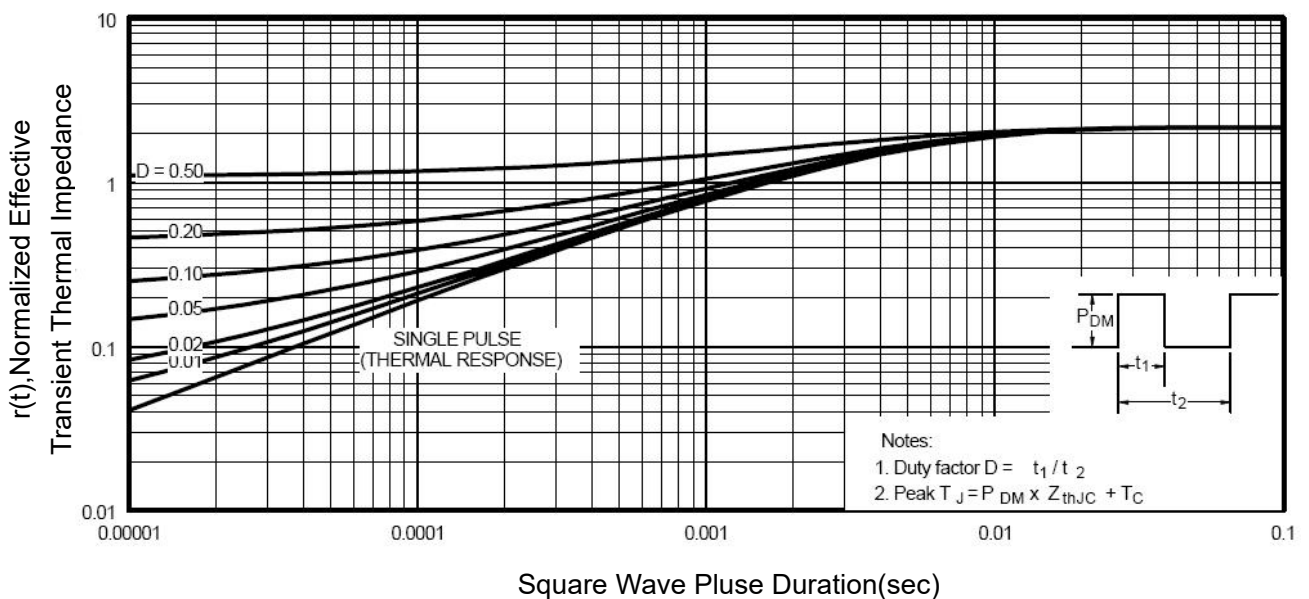
**Figure 8 Safe Operation Area**



**Figure 9 BV<sub>DSS</sub> vs Junction Temperature**

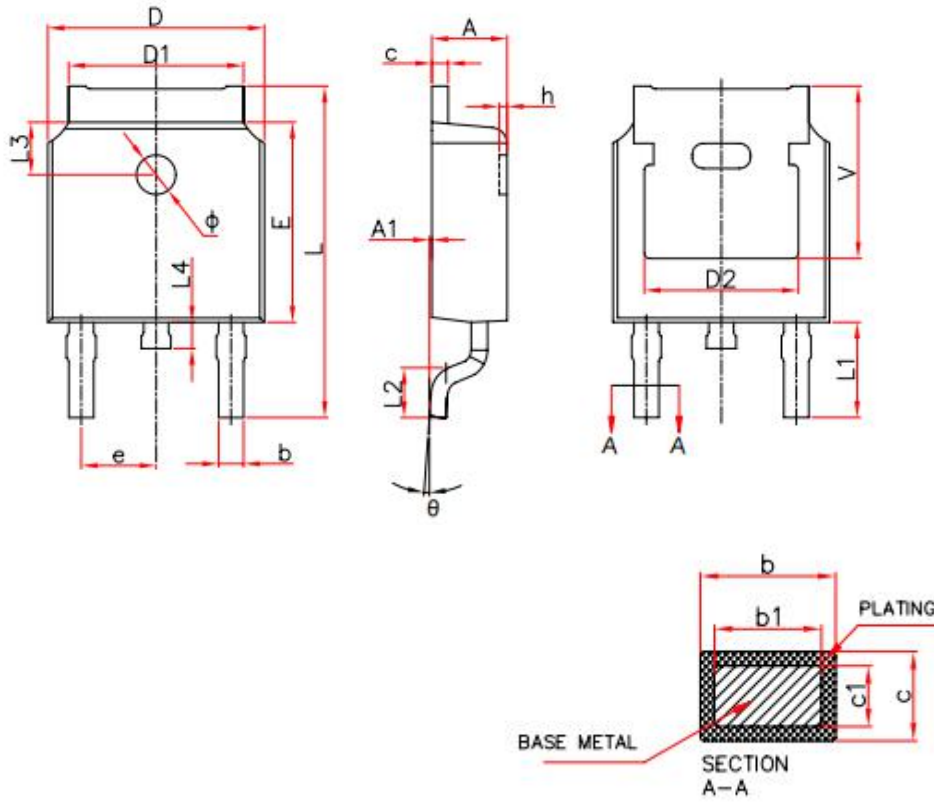


**Figure 10 V<sub>GS(th)</sub> vs Junction Temperature**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

## TO-252-2L Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
Φ	1.10	1.30
θ	0°	8°
h	0.00	0.30
V	5.35 REF.	

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