

NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE02P20K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

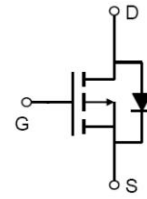
General Features

- $V_{DS} = -200V, I_D = -20A$
 $R_{DS(ON)} < 200m\Omega @ V_{GS} = -10V$ (Typ: 183m Ω)
 $R_{DS(ON)} < 240m\Omega @ V_{GS} = -4.5V$ (Typ: 188m Ω)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

Application

- Portable equipment and battery powered systems

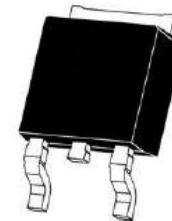
100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE02P20K	NCE02P20K	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-200	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	-20	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D (100^\circ C)$	-14.1	A
Pulsed Drain Current	I_{DM}	-80	A
Maximum Power Dissipation	P_D	180	W
Single pulse avalanche energy (Note 5)	E_{AS}	282	mJ
Derating factor		1.2	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	0.83	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	$^\circ C/W$

Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

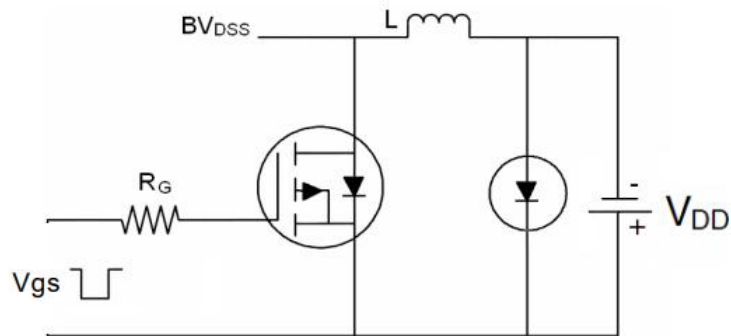
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-200	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-200V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.2	-1.8	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-15A	-	183	200	mΩ
		V _{GS} =-4.5V, I _D =-15A	-	188	220	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-20A	-	50	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{iss}	V _{DS} =-100V, V _{GS} =0V, F=1.0MHz	-	6596	-	pF
Output Capacitance	C _{Oss}		-	82	-	pF
Reverse Transfer Capacitance	C _{rss}		-	59	-	pF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-100V, I _D =-20A V _{GS} =-10V, R _{GEN} =5Ω	-	17	-	nS
Turn-on Rise Time	t _r		-	80	-	nS
Turn-Off Delay Time	t _{d(off)}		-	45	-	nS
Turn-Off Fall Time	t _f		-	65	-	nS
Total Gate Charge	Q _g	V _{DS} =-100V, I _D =-20A, V _{GS} =-10V	-	122	-	nC
Gate-Source Charge	Q _{gs}		-	19	-	nC
Gate-Drain Charge	Q _{gd}		-	22	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =-20A	-	-	-1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S	-	-	-	-20	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =-20A di/dt = 100A/μs ^(Note3)	-	90	-	nS
Reverse Recovery Charge	Q _{rr}		-	145	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

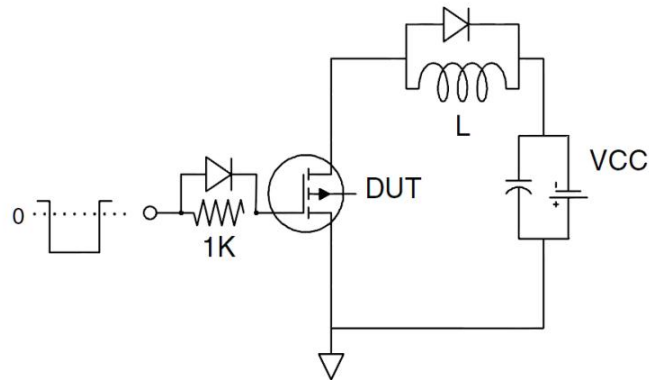
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, L=0.5mH, R_g=25\Omega$

Test Circuit

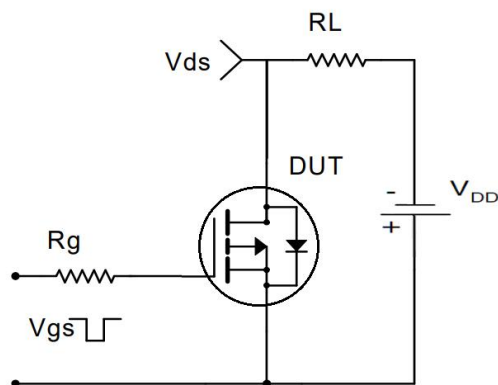
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

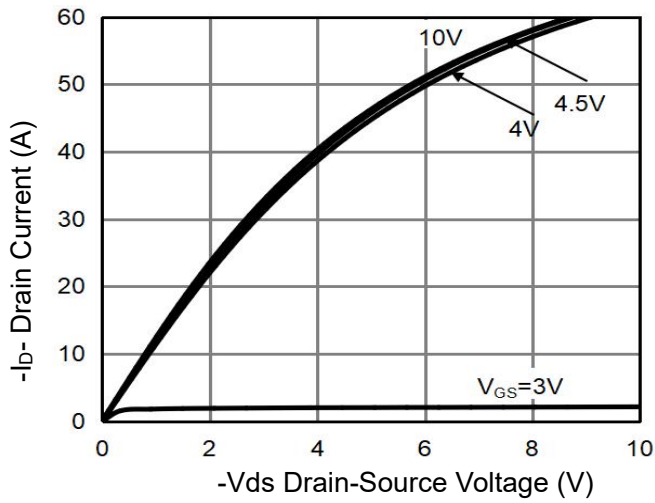


Figure 1 Output Characteristics

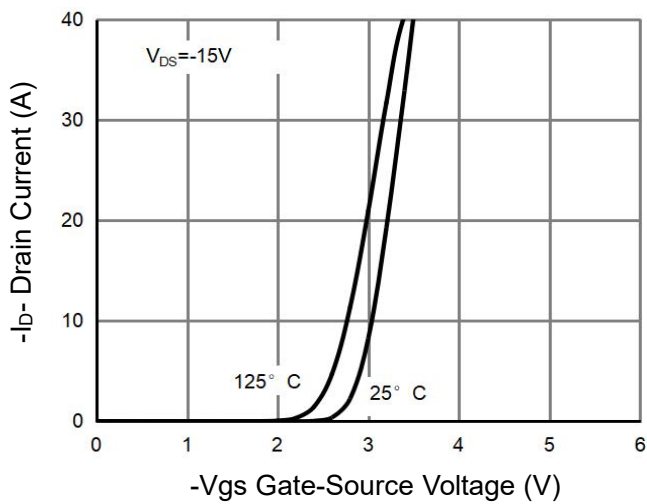


Figure 2 Transfer Characteristics

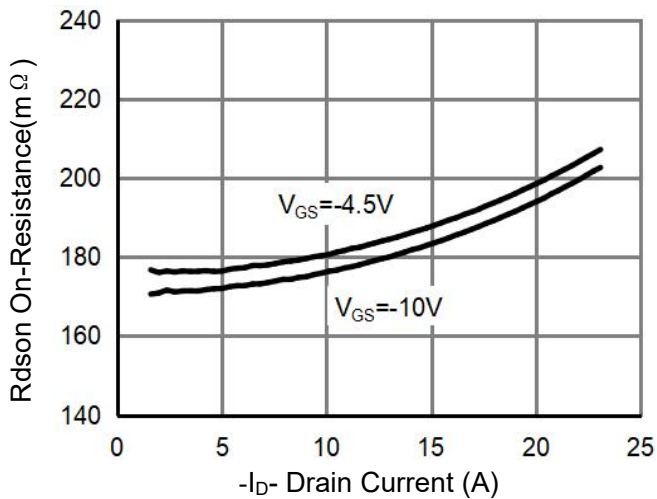


Figure 3 Rdson- Drain Current

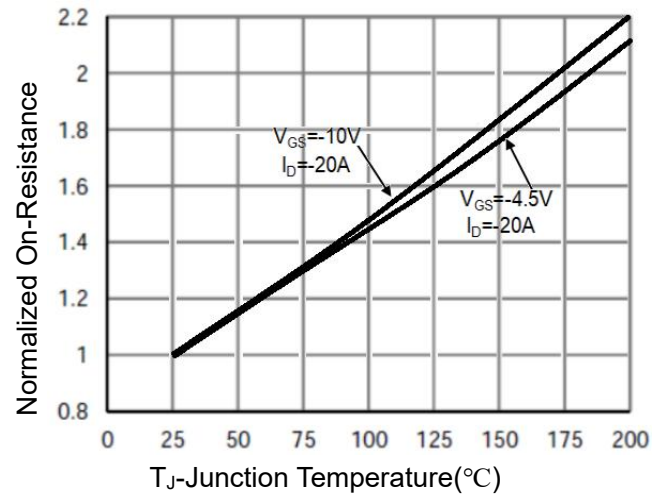


Figure 4 Rdson-Junction Temperature

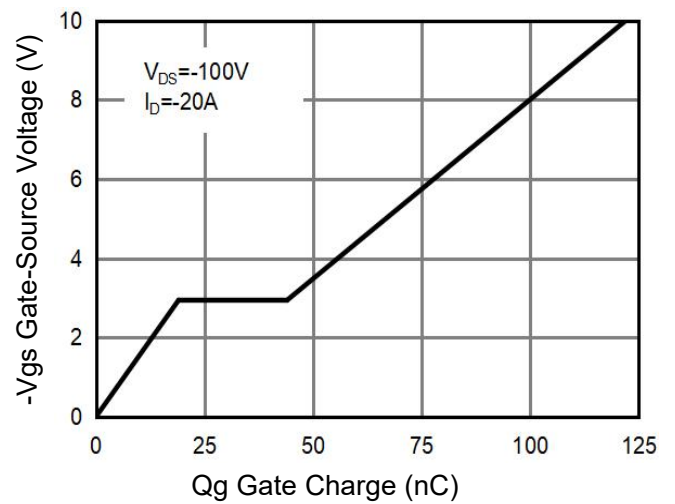


Figure 5 Gate Charge

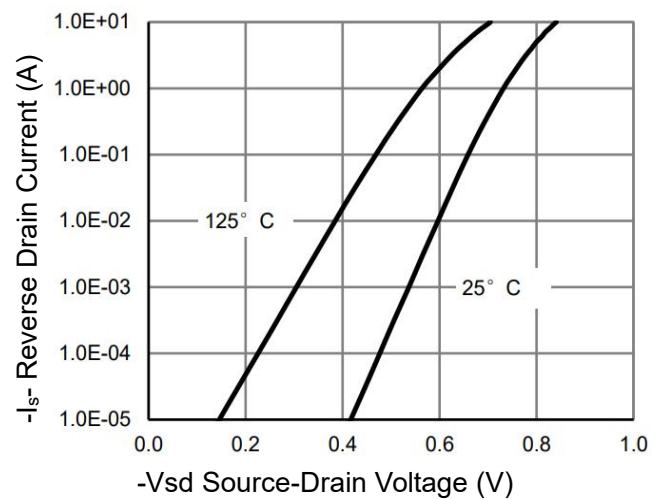


Figure 6 Source- Drain Diode Forward

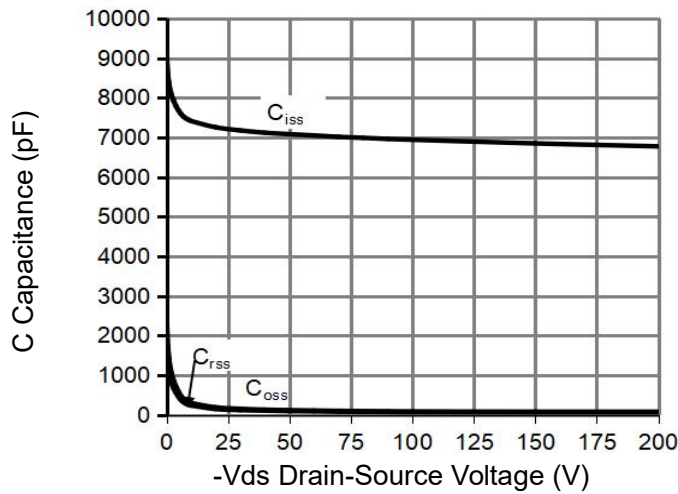


Figure 7 Capacitance vs Vds

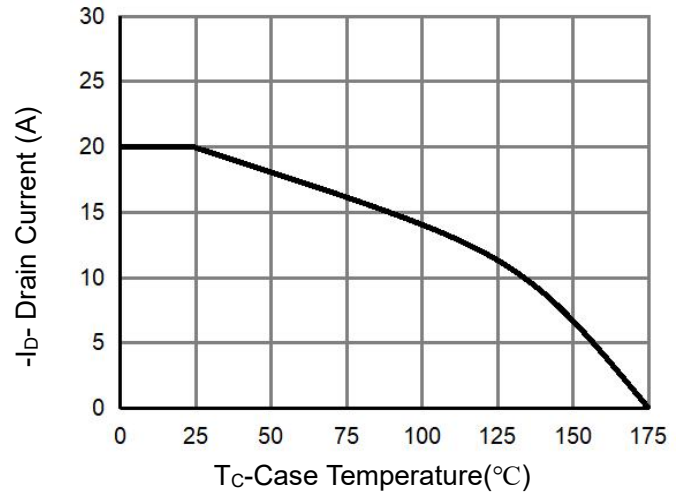


Figure 9 Drain Current vs Case Temperature

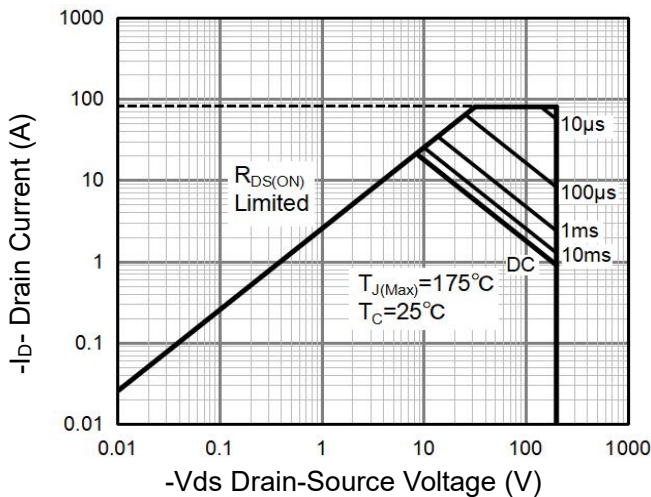


Figure 8 Safe Operation Area

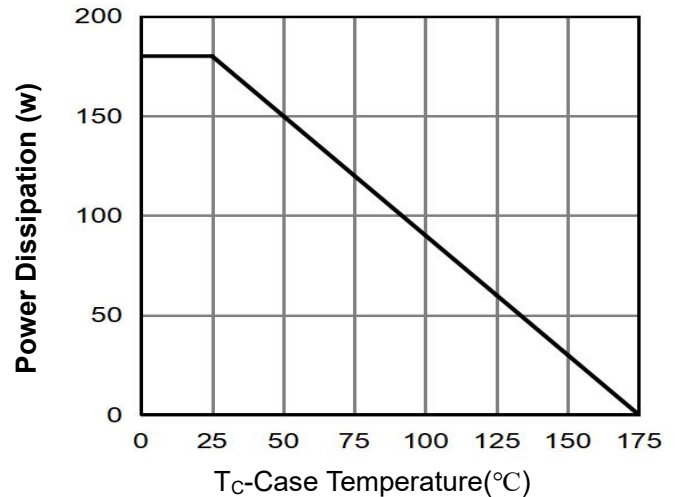


Figure 10 Power De-rating

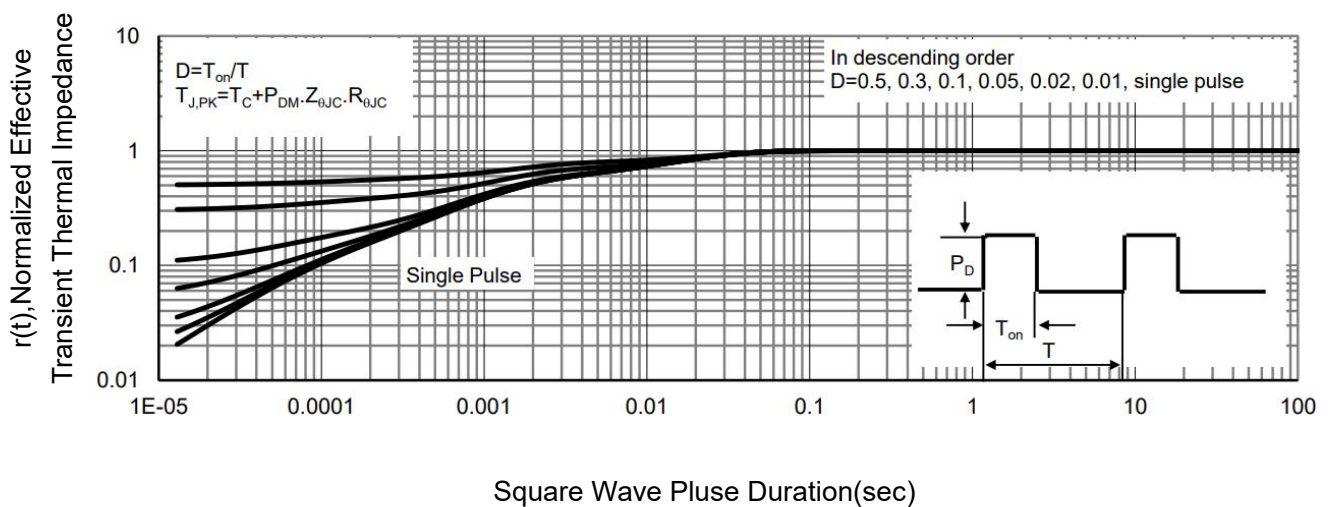
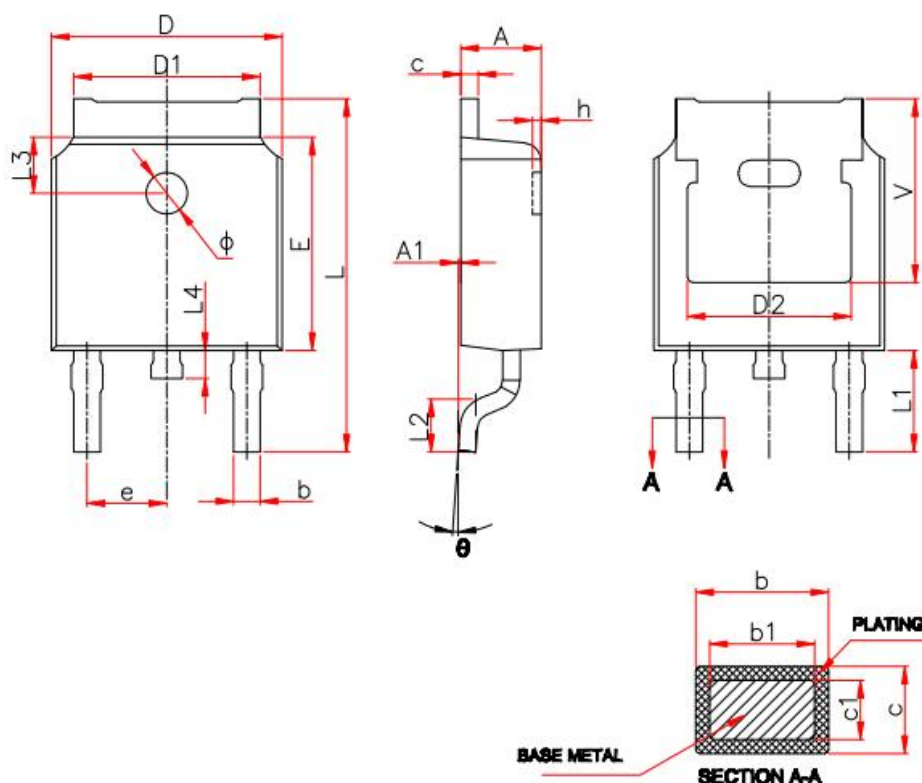


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
ϕ	1.10	1.30
θ	0°	8°
h	0.00	0.30
V	5.35 REF.	

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