NCE Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

Description

The NCE1230SP uses advanced trench technology to provide excellent $R_{SS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V $V_{GS(MAX)}$ rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

Application

- Lithium-ion battery charging and discharging switch

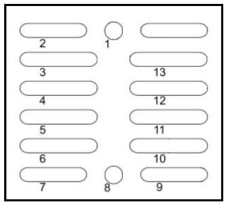
General Features

- V_{SSS} =12V,I_S =30A
  $R_{SS(on)}$=1.0mΩ (typical) @ V_{GS}=4.5V
  $R_{SS(on)}$=1.4mΩ (typical) @ V_{GS}=2.5V
- 2.5V drive
- Common-drain type
- 2KV HBM

Package Information

- Minimum Packing Quantity : 3,000 pcs./reel

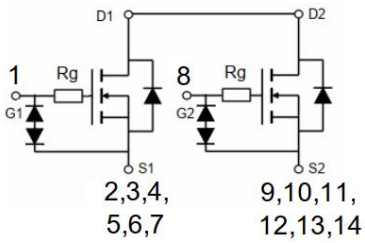
CSP3.0X2.74



1. Gate1 (FET1) 2,3,4,5,6,7. Source1 (FET1)
8. Gate2 (FET2) 9,10,11,12,13,14. Source2 (FET2)

Bottow View

Schematic Diagram



Absolute Maximum Ratings (T_A =25℃unless otherwise noted)

Symbol	Parameter	Limit	Unit
V_{SSS}	Source to Source Voltage	12	V
V_{GSS}	Gate-Source Voltage	±8	V
I_S	Source Current(DC)	30	A
I_{SP}	Source Current (Pulse)	200	A
P_T	Total Dissipation (Note 1)	4.0	W
Tch	Channel Temperature	150	℃
T_{STG}	Storage Temperature	-55 To 150	℃

Electrical Characteristics (T_A=25℃unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
BV_{SSS}	Source to Source Breakdown Voltage	I_S=1mA, V_{GS}=0V, Test Circuit 1	12	-	-	V
I_{SSS}	Zero- Gate Voltage Source Current	V_{SS}=12V V_{GS}=0V, Test Circuit 1	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{SS}=0V, V_{GS}= ±8V, Test Circuit 2	-	-	±10	μA

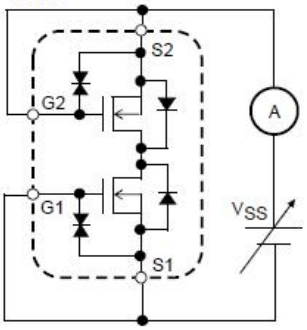
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{GS(off)}$	Cutoff Voltage	V_{SS}=6V, I_S=1mA, Test Circuit 3	0.5	0.9	1.3	V
$\|yg_{FS}\|$	Forward Transfer Admittance	V_{SS}=6V,I_S=10A, Test Circuit 4	-	25	-	S
$R_{SS(on)}$	Static Source to Source On-Resistance	V_{GS}=4.5V,I_S=10A, Test Circuit 5	0.7	1.0	1.3	mΩ
		V_{GS}=3.8,I_S=10A, Test Circuit 5	0.75	1.1	1.45	mΩ
		V_{GS}=3.1V,I_S=10A, Test Circuit 5	0.85	1.3	2.0	mΩ
		V_{GS}=2.5V,I_S=10A, Test Circuit 5	0.9	1.4	3.0	mΩ
$t_{d(on)}$	Turn-on Delay Time	V_{SS}=10V,I_S=10A V_{GS}=4.5V Test Circuit 7	-	2500	-	nS
t_r	Turn-on Rise Time		-	4000	-	nS
$t_{d(off)}$	Turn-Off Delay Time		-	9700	-	nS
t_f	Turn-Off Fall Time		-	5800	-	nS
Qg	Total Gate Charge	V_{SS}=6V,I_S=10A,V_{GS}=4.5V Test Circuit 8	-	84.3	-	nC
Qgs	Gate-Source Charge		-	8.2	-	nC
Qgd	Gate-Drain Charge		-	21.5	-	nC
C_{lss}	Input Capacitance	V_{SS}=10V,V_{GS}=0V, F=1.0KHz	-	7510	-	PF
C_{oss}	Output Capacitance		-	944	-	PF
C_{rss}	Reverse Transfer Capacitance		-	831	-	PF
R_G	Gate resistance	F=1.0KHz	-	645	-	Ω
$V_{F(S-S)}$	Diode Forward Voltage	V_{GS}=0V,I_S=10A	-	-	1.2	V

Notes:

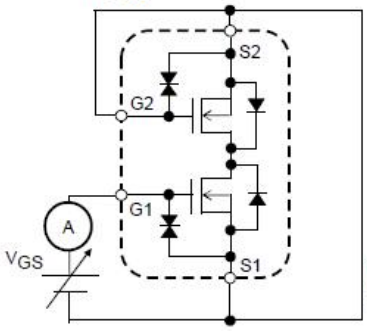
1 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm). t = 10 μs, Duty Cycle ≤ 1 %

Test Circuit

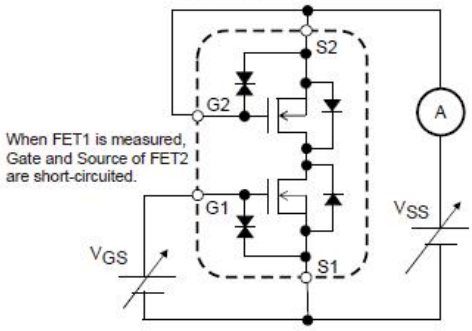
Test Circuit 1
I_{SSS}



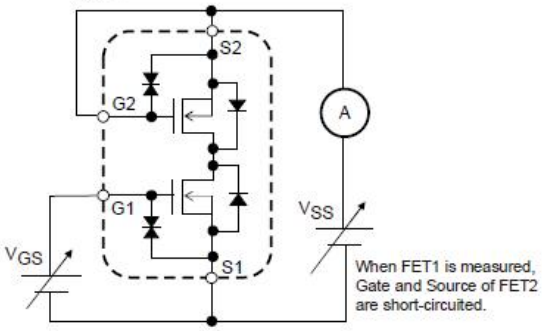
Test Circuit 2
I_{GSS}



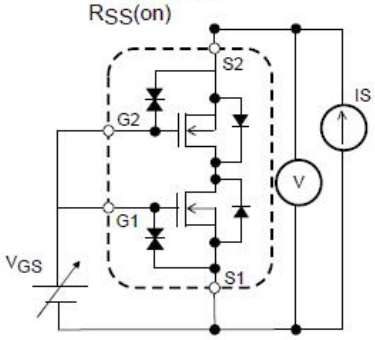
Test Circuit 3
$V_{GS(off)}$



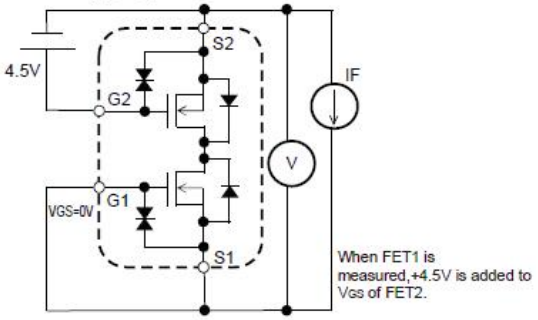
Test Circuit 4
$|y_{fs}|$



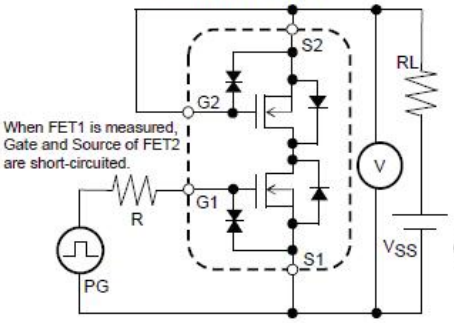
Test Circuit 5
$R_{SS(on)}$



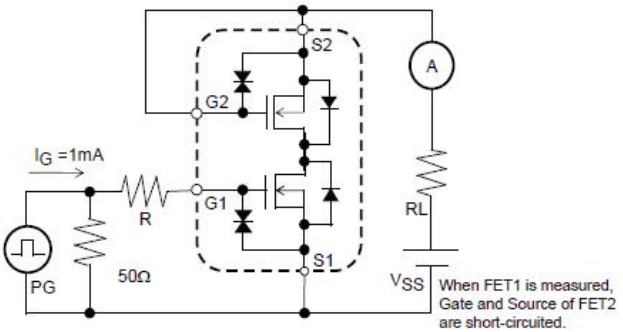
Test Circuit 6
$V_{F(S-S)}$



Test Circuit 7
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f



Test Circuit 8
Qg



Typical Electrical and Thermal Characteristics (Curves)

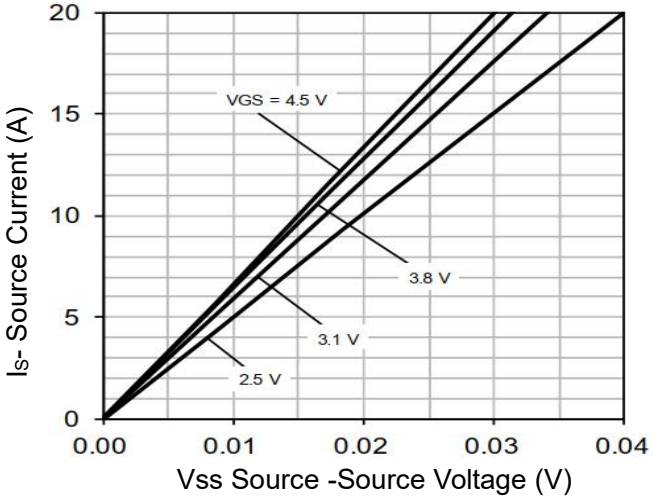


Figure 1 On-Region Characteristics

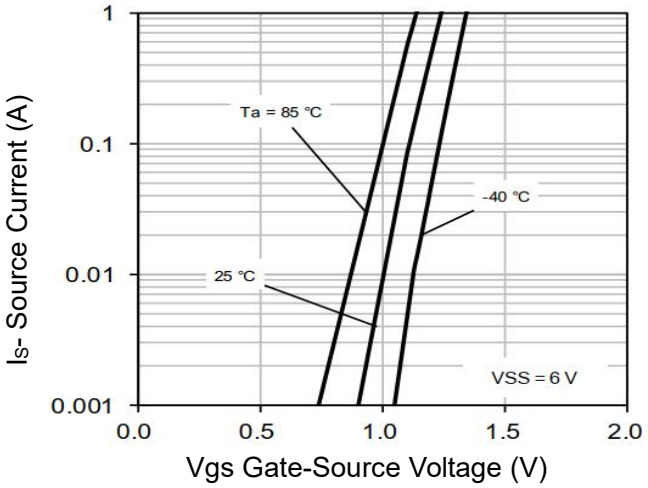


Figure 2 Transfer Characteristics

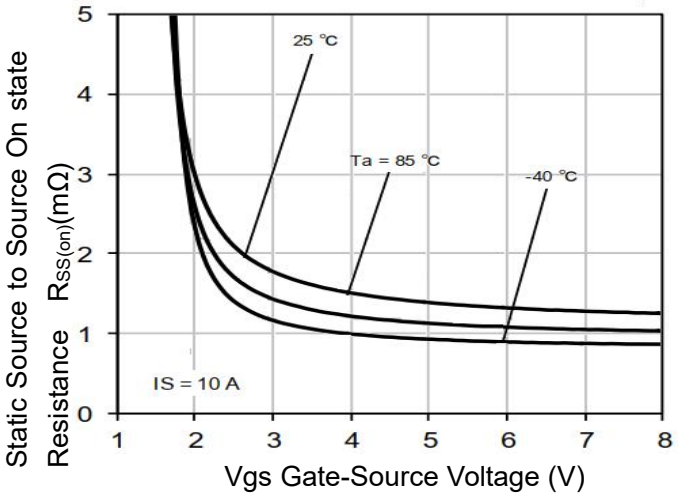


Figure3 On-Resistance-Gate-Source Voltage

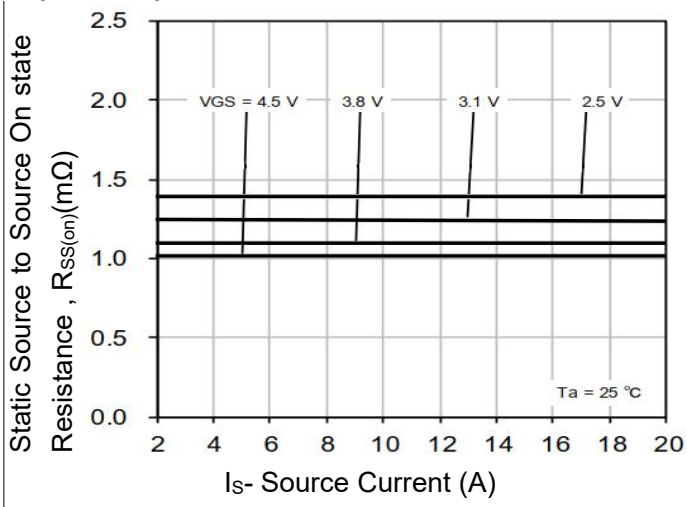


Figure 4 Rss(on)- Source Current

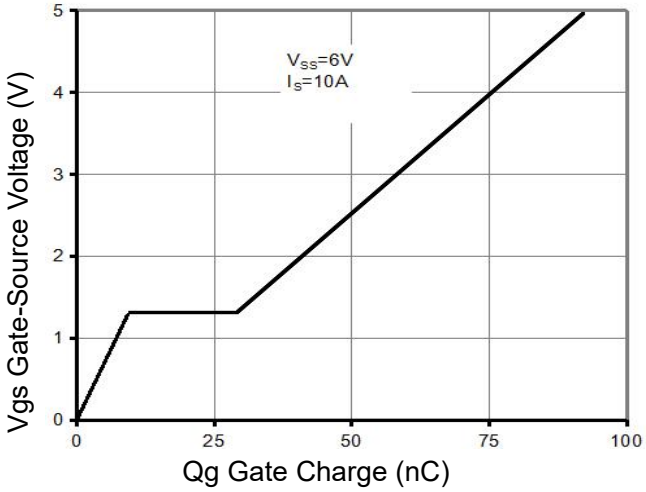


Figure 5 Gate Charge

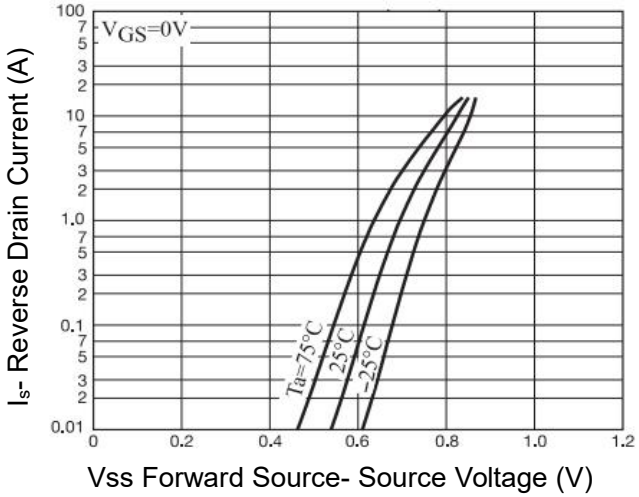


Figure 6 Body-Diode Characteristics

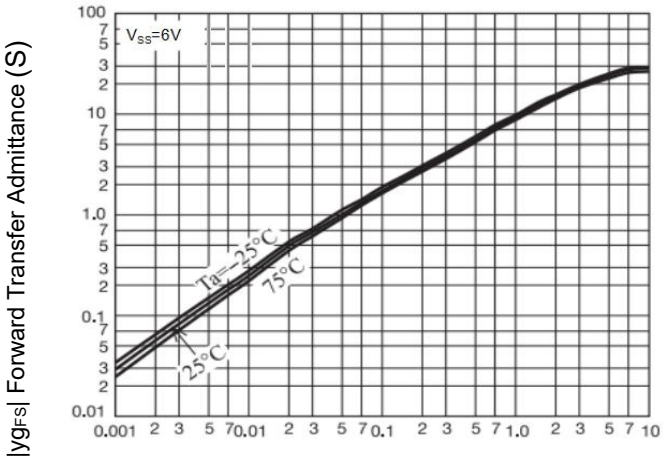


Figure7 |yfs|-- I_S

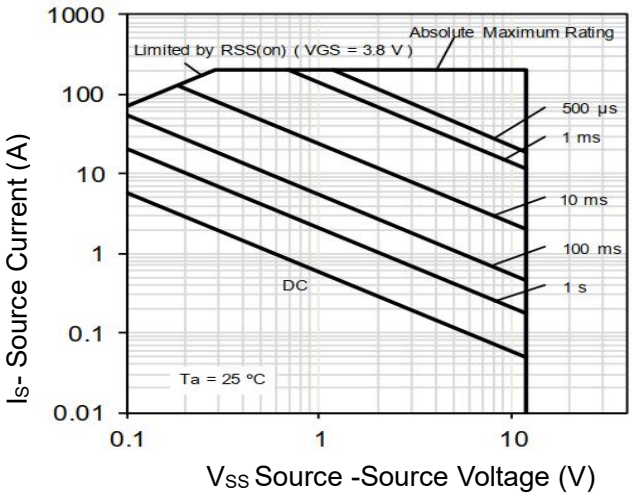


Figure 8 Safe Operation Area

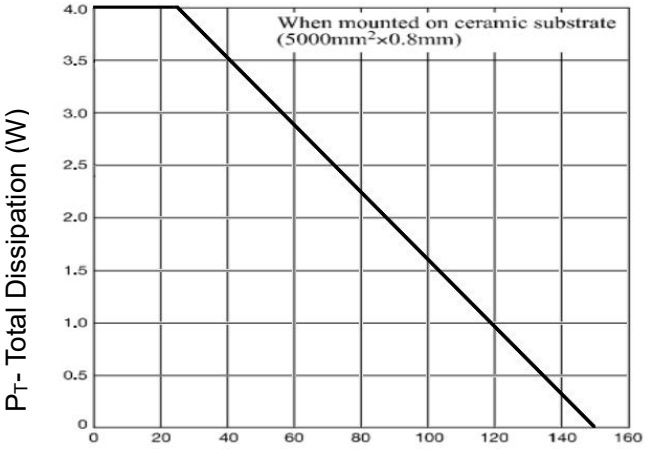


Figure 9 P_T Dissipation De-rating

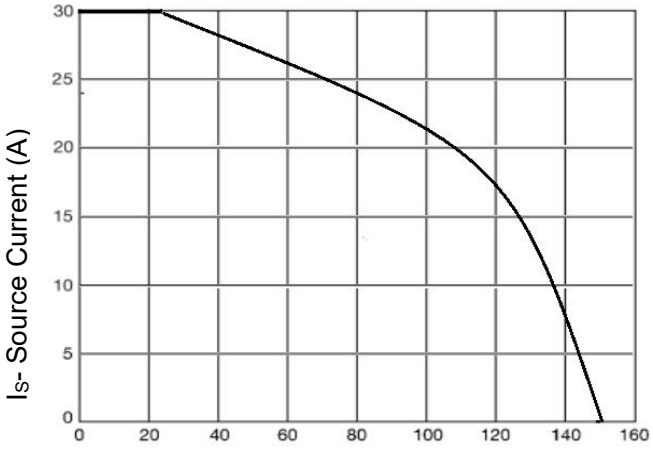


Figure 10 Current De-rating

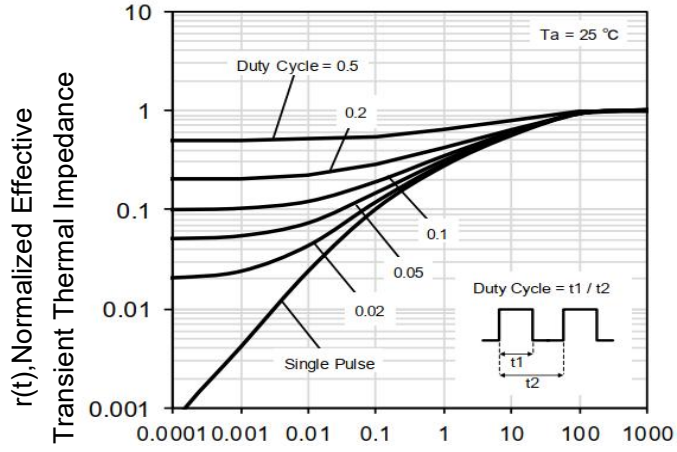
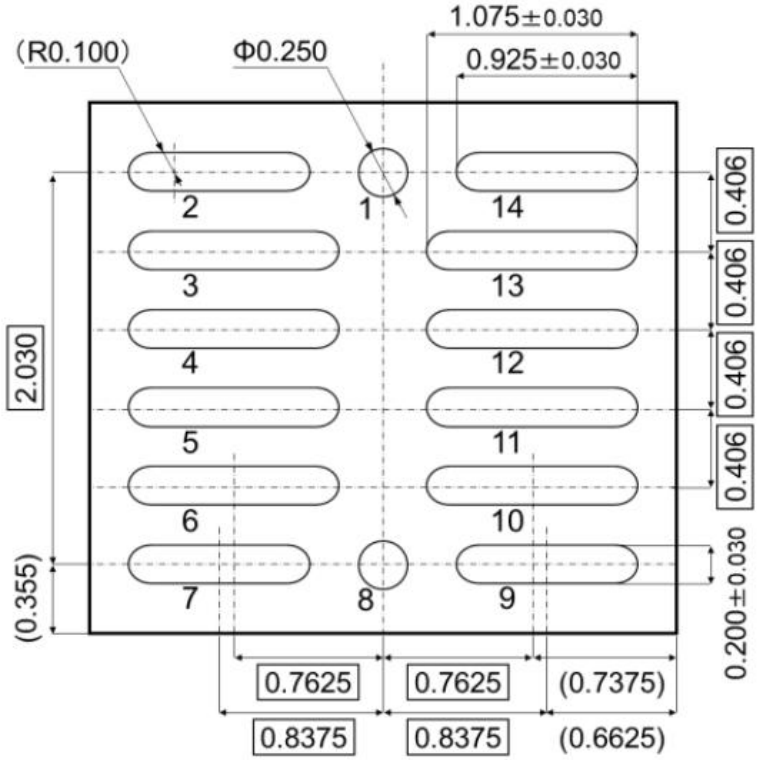


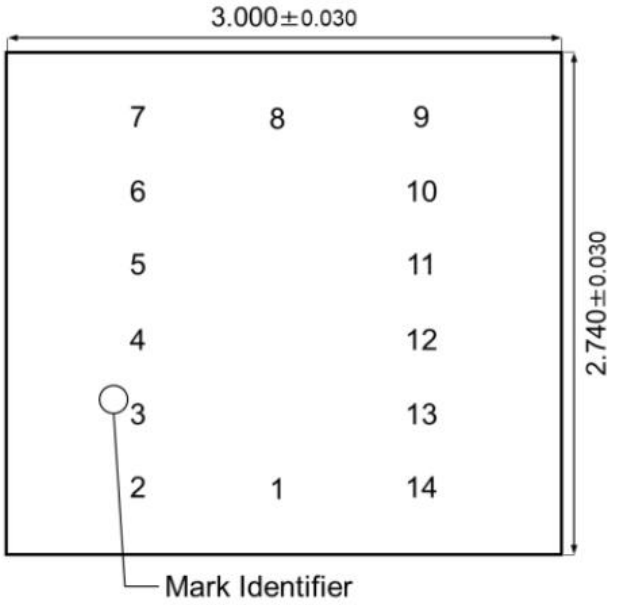
Figure 11 Normalized Maximum Transient Thermal Impedance

Package Dimensions

(Bottom View)



(Top View)



(Front View)

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