

NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE20P85GU uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

- Load switch
- Battery protection

100% UIS TESTED!

100% ΔV_{ds} TESTED!

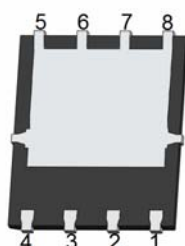
General Features

- $V_{DS} = -20V, I_D = -85A$
 $R_{DS(ON)} < 1.9m\Omega @ V_{GS} = -4.5V$
 $R_{DS(ON)} < 2.4m\Omega @ V_{GS} = -2.5V$
 $R_{DS(ON)} < 3.8m\Omega @ V_{GS} = -1.8V$
- High density cell design for ultra low $R_{ds(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

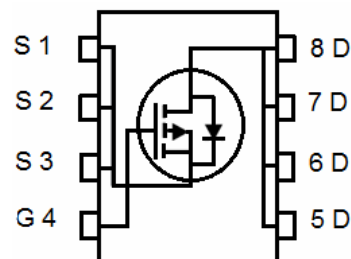
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
20P85GU	NCE20P85GU	DFN 5x6 -8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous	I_D	-85	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	-60.1	A
Pulsed Drain Current	I_{DM}	-340	A
Maximum Power Dissipation	P_D	150	W
Single pulse avalanche energy ^(Note 5)	E_{AS}	420	mJ
Derating factor		1.2	W/ $^\circ C$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.83	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-20V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.4	-0.6	-1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=-4.5V, I_D=-20A$	-	1.4	1.9	m Ω
		$V_{GS}=-2.5V, I_D=-20A$	-	1.9	2.4	
		$V_{GS}=-1.8V, I_D=-20A$		2.6	3.8	
Forward Transconductance	g_{FS}	$V_{DS}=-5V, I_D=-20A$	105	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{ISS}	$V_{DS}=-10V, V_{GS}=0V,$ $F=1.0MHz$	-	12670	-	PF
Output Capacitance	C_{OSS}		-	1695	-	PF
Reverse Transfer Capacitance	C_{RSS}		-	1485	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=-10V, R_{GEN}=3\Omega$ $V_{GS}=-4.5V, R_L=0.5\Omega$	-	16	-	nS
Turn-on Rise Time	t_r		-	38	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	360	-	nS
Turn-Off Fall Time	t_f		-	210	-	nS
Total Gate Charge	Q_g	$V_{DS}=-10V, I_D=-20A,$ $V_{GS}=-4.5V$	-	114.7	-	nC
Gate-Source Charge	Q_{gs}		-	22.4	-	nC
Gate-Drain Charge	Q_{gd}		-	23.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=-20A$	-	-	-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-85	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = -10A$ $di/dt = 100A/\mu s^{(Note3)}$	-	150	-	nS
Reverse Recovery Charge	Q_{rr}		-	240	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=-10V, V_G=-10V, L=0.5\text{mH}, R_g=25\Omega$

Typical Electrical and Thermal Characteristics (Curves)

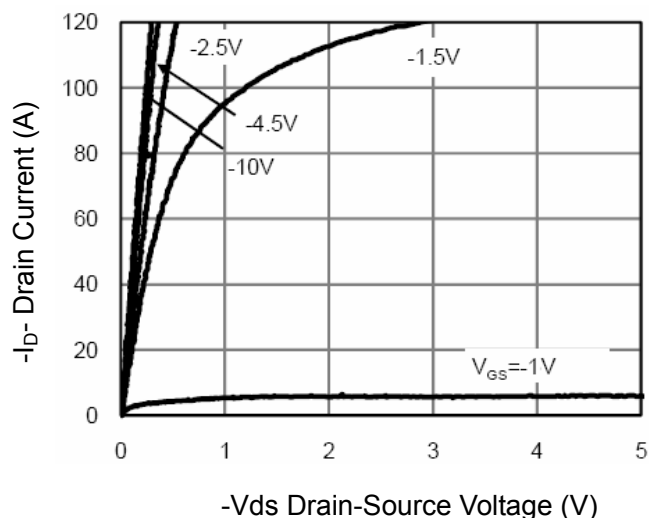


Figure 1 Output Characteristics

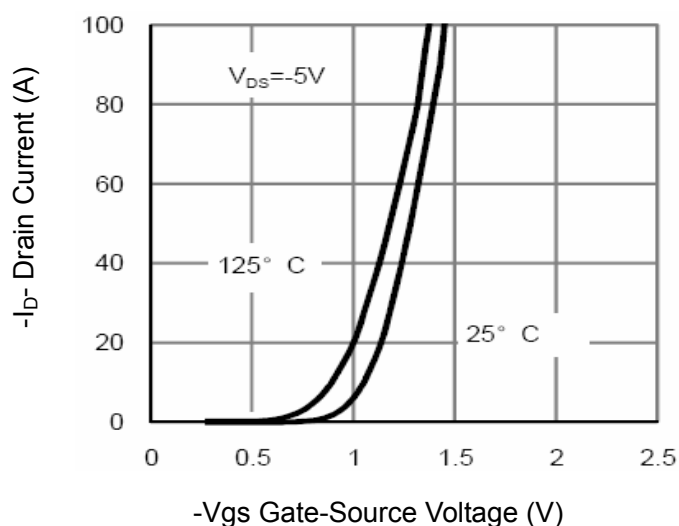


Figure 2 Transfer Characteristics

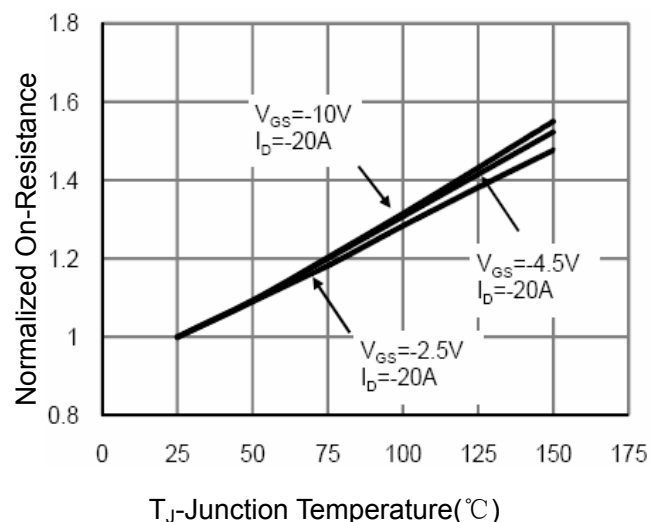


Figure 4 Rdson-Junction Temperature

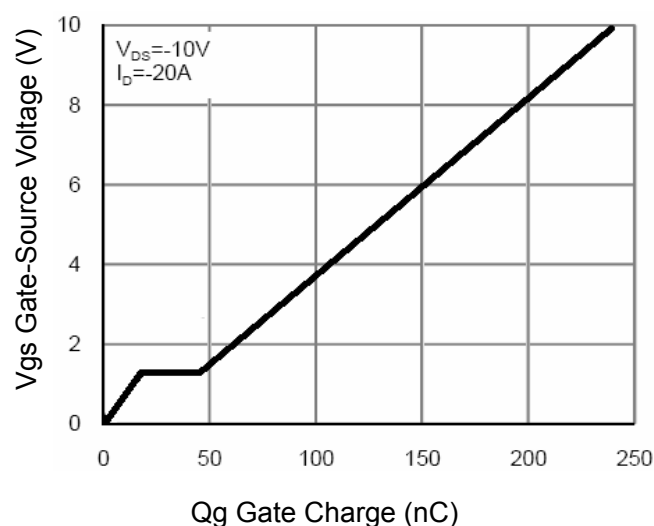


Figure 5 Gate Charge

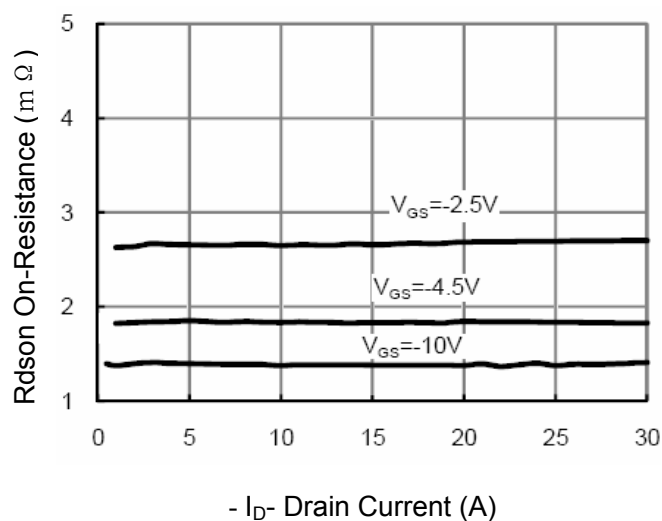


Figure 3 Rdson- Drain Current

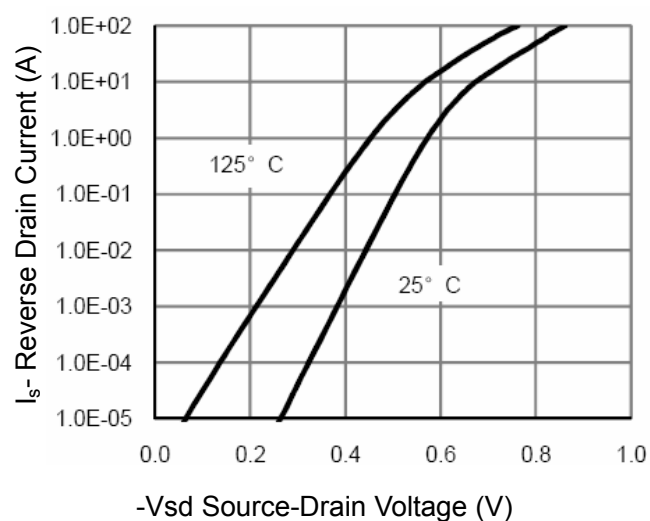
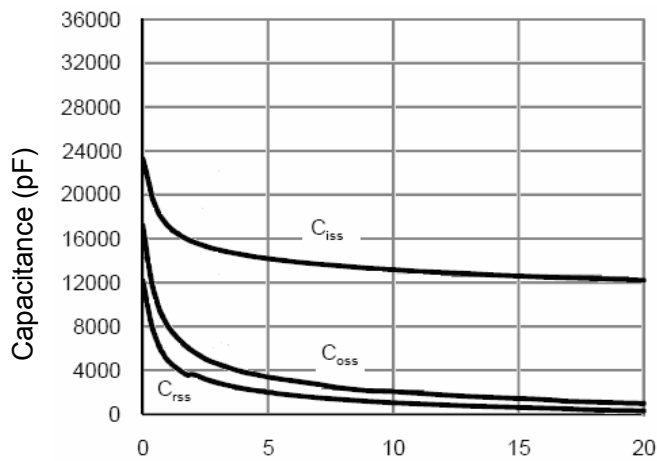
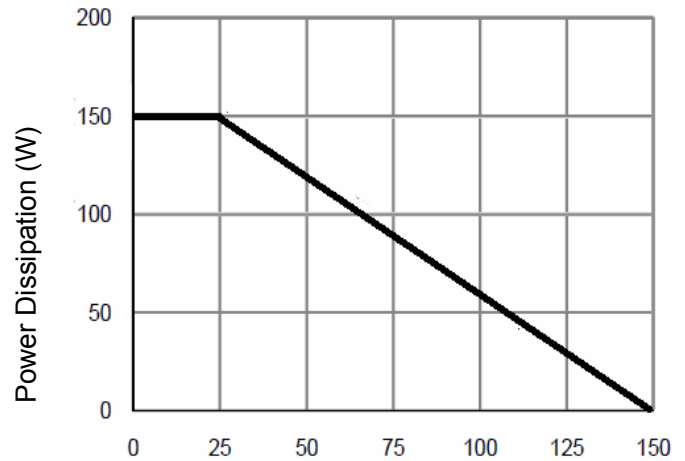


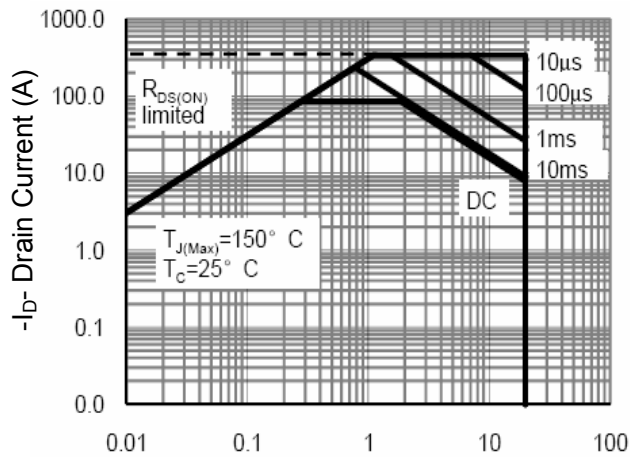
Figure 6 Source- Drain Diode Forward



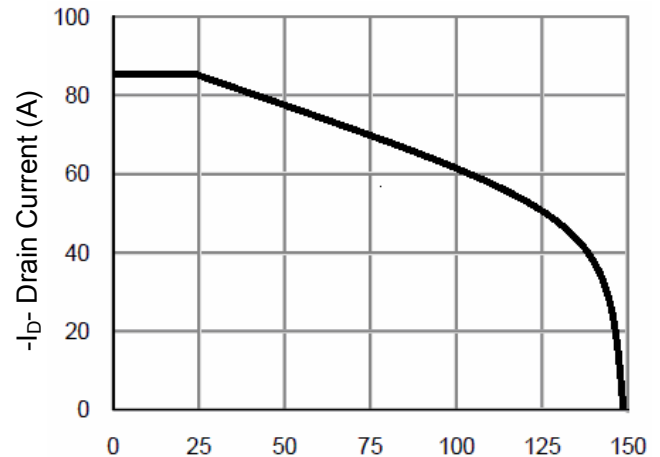
-Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 Power De-rating



-Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)
Figure 10 -Current De-rating

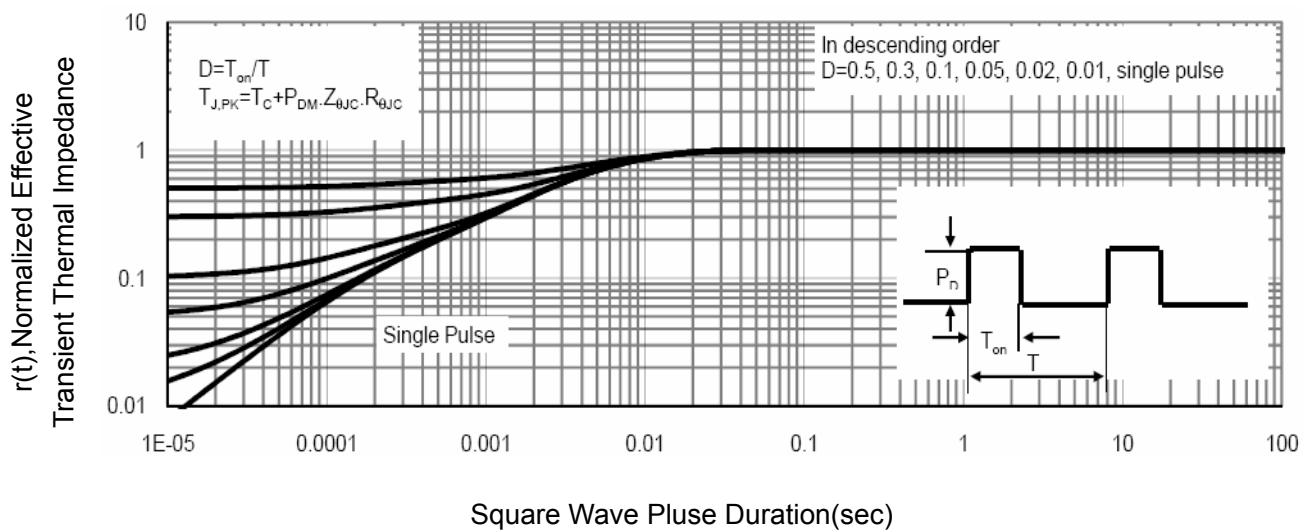
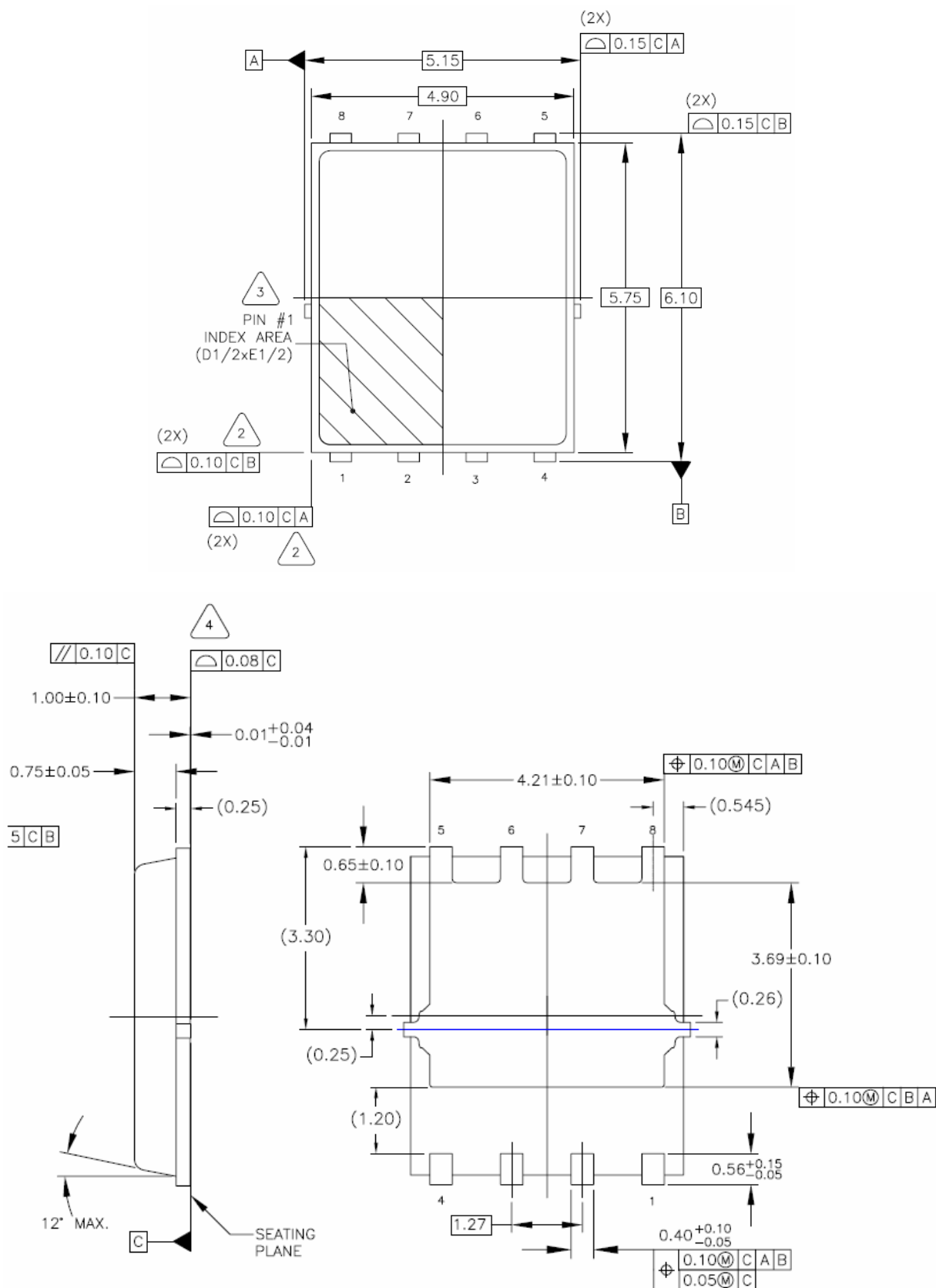


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



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