

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE3068Q uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

Application

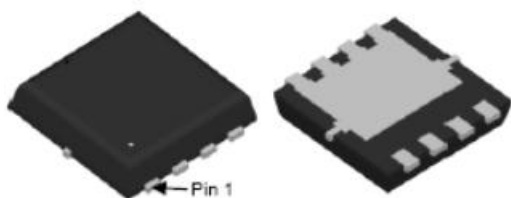
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!
100% ΔV_{ds} TESTED!

General Features

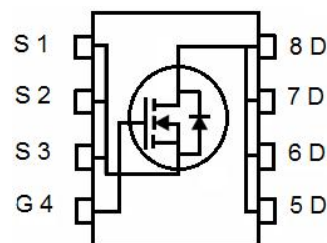
- $V_{DS} = 30V, I_D = 68A$
- $R_{DS(ON)} = 3.5m\Omega$ (max) @ $V_{GS} = 10V$
- $R_{DS(ON)} = 6.2m\Omega$ (max) @ $V_{GS} = 4.5V$
- High density cell design for ultra low R_{dson}
- Very low on-resistance $R_{DS(on)}$
- Good stability and uniformity with high E_{AS}
- 150 °C operating temperature
- Pb-free lead plating

PDFN 3.3X3.3-8L



Top View

Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE3068Q	NCE3068Q	PDFN 3.3X3.3-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	68	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	48	A
Pulsed Drain Current (Note 1)	I_{DM}	272	A
Maximum Power Dissipation	P_D	45	W
Derating factor		0.36	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	150	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.78	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	60	$^\circ C/W$

Electrical Characteristics (TC=25°C unless otherwise noted)

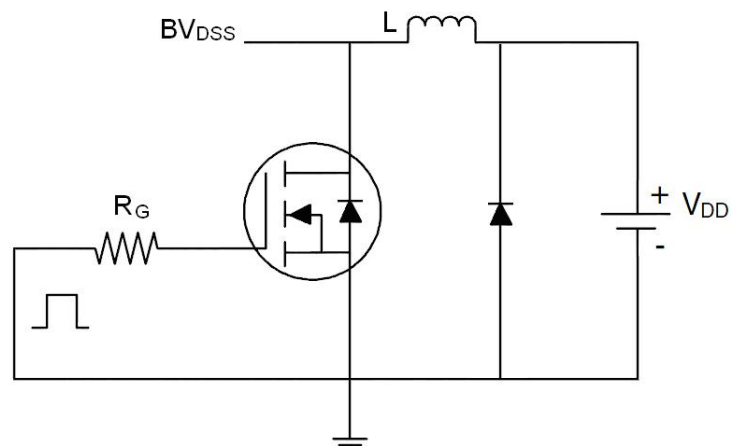
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.5	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.5	4.1	mΩ
		V _{GS} =4.5V, I _D =20A	-	6.2	7.5	
Gate resistance	R _G	V _{DS} =0V, V _{GS} =0V, F=1.0MHz	-	1.9	-	Ω
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	-	30	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{ISS}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	1784	-	pF
Output Capacitance	C _{OSS}		-	266	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	212	-	pF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =5V, I _D =20A V _{GS} =10V, R _{GEN} =6Ω	-	7	-	nS
Turn-on Rise Time	t _r		-	6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	30	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =20A, V _{GS} =10V	-	38.4	-	nC
Gate-Source Charge	Q _{gs}		-	5.8	-	nC
Gate-Drain Charge	Q _{gd}		-	7.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =20A	-	0.85	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	68	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs <small>(Note3)</small>	-	47	-	nS
Reverse Recovery Charge	Q _{rr}		-	47	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

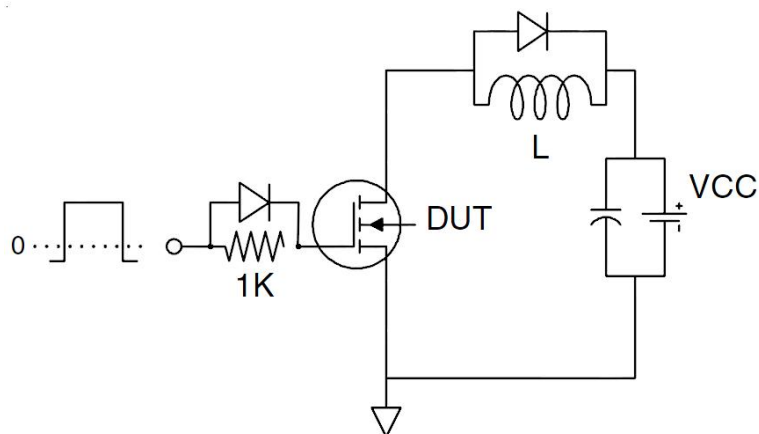
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz.Copper, in a still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ C, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

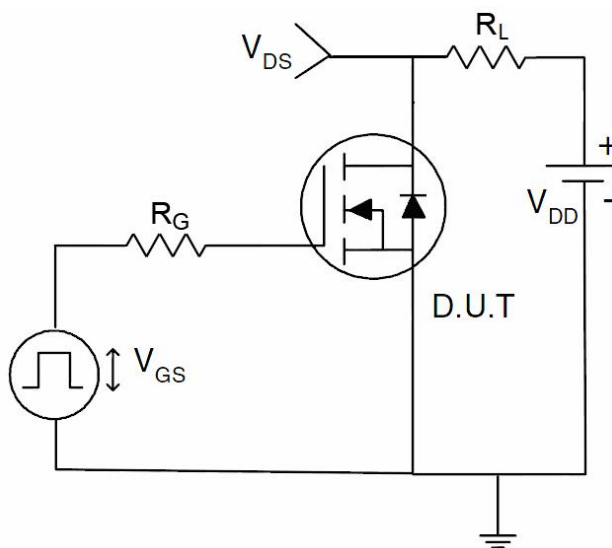
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

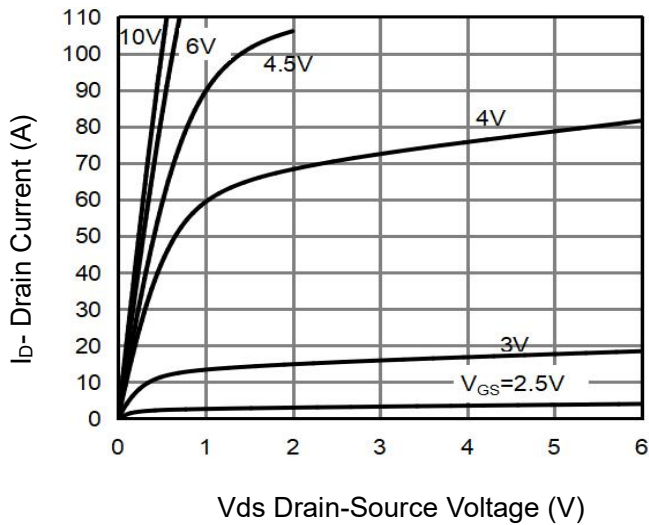


Figure 1 Output Characteristics

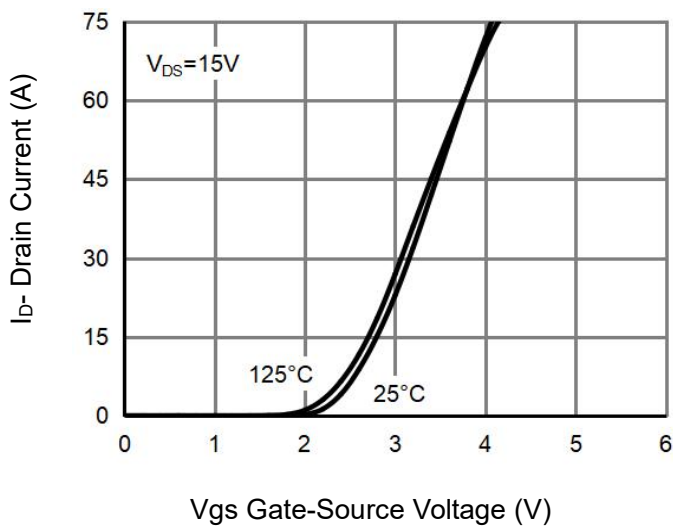


Figure 2 Transfer Characteristics

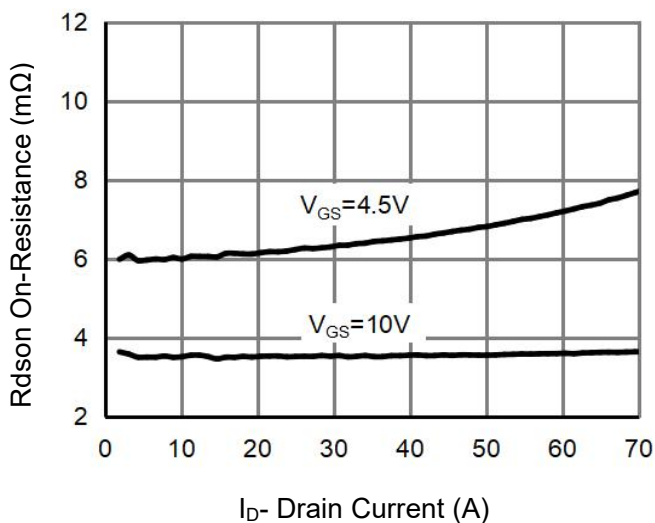


Figure 3 $R_{DS(on)}$ - Drain Current

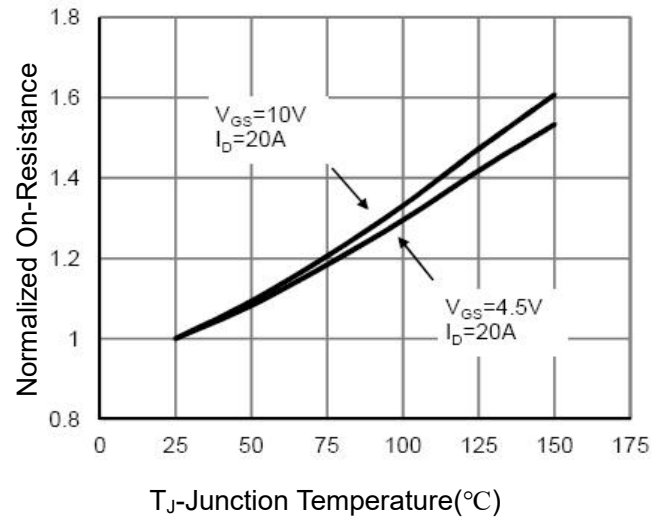


Figure 4 $R_{DS(on)}$ -Junction Temperature

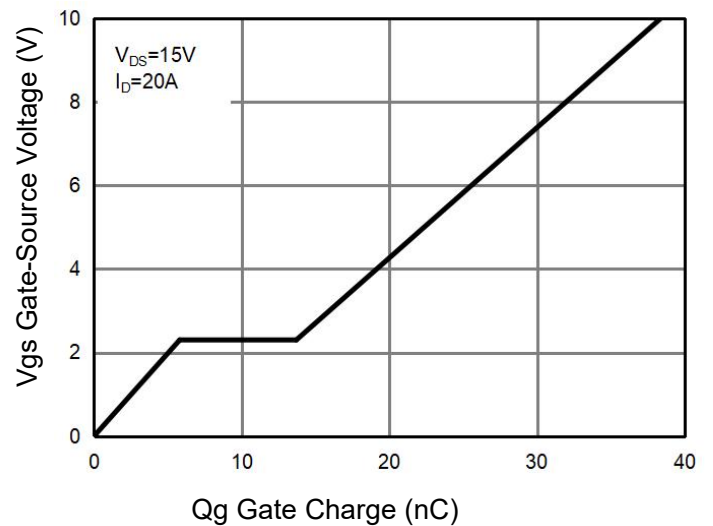


Figure 5 Gate Charge

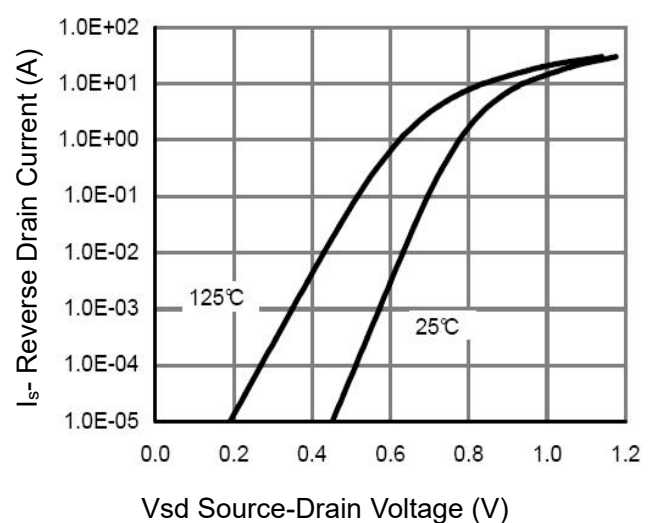
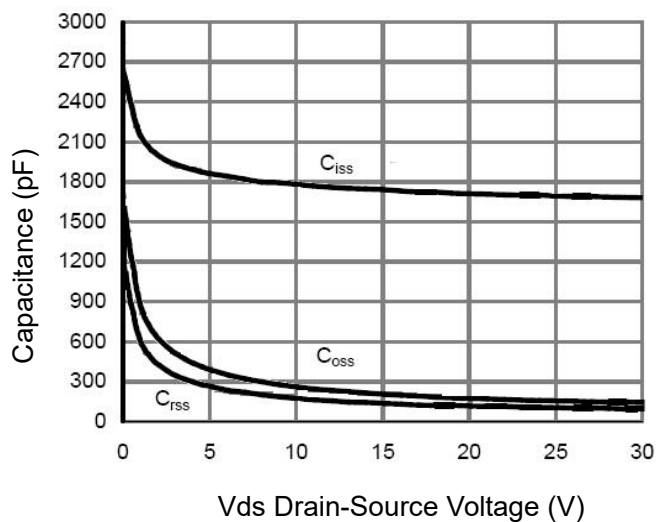
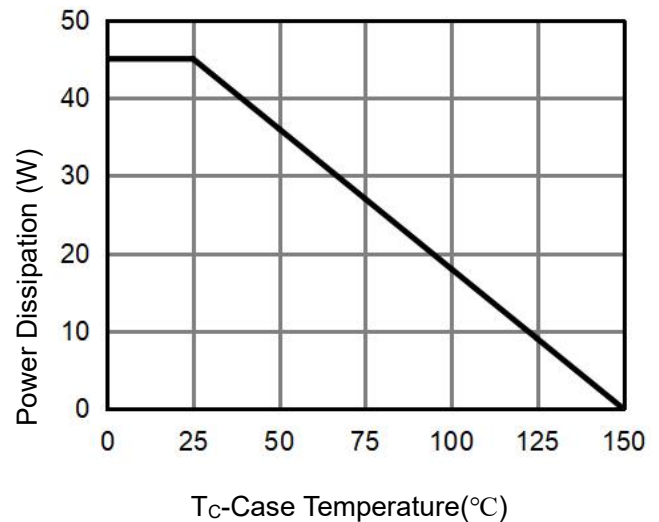


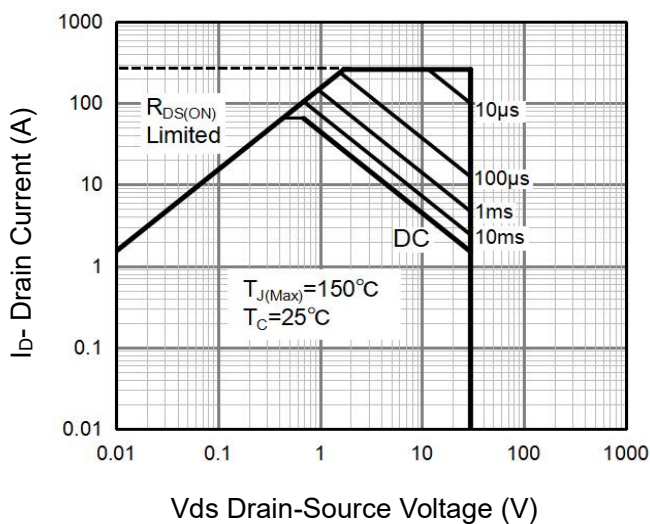
Figure 6 Source- Drain Diode Forward



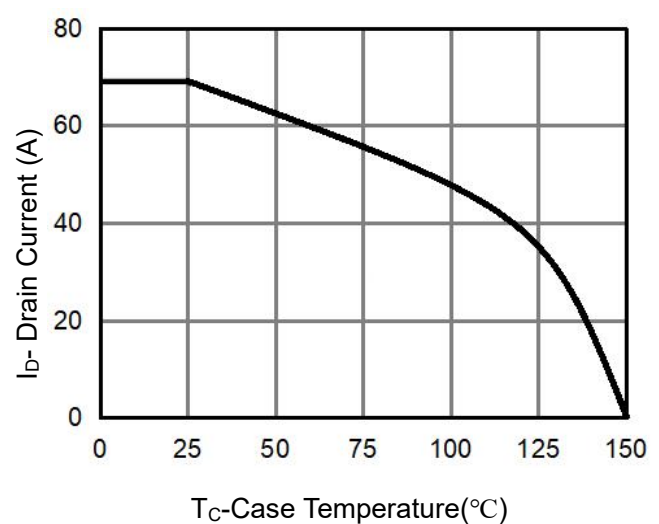
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



Tc-Case Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



Tc-Case Temperature(°C)
Figure 10 Current De-rating

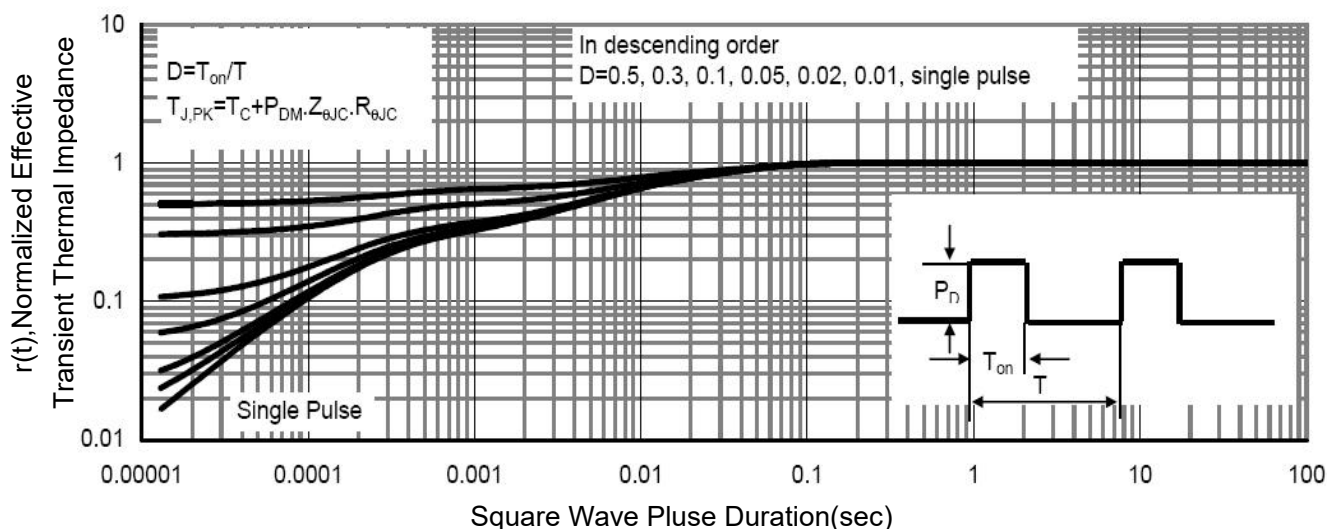
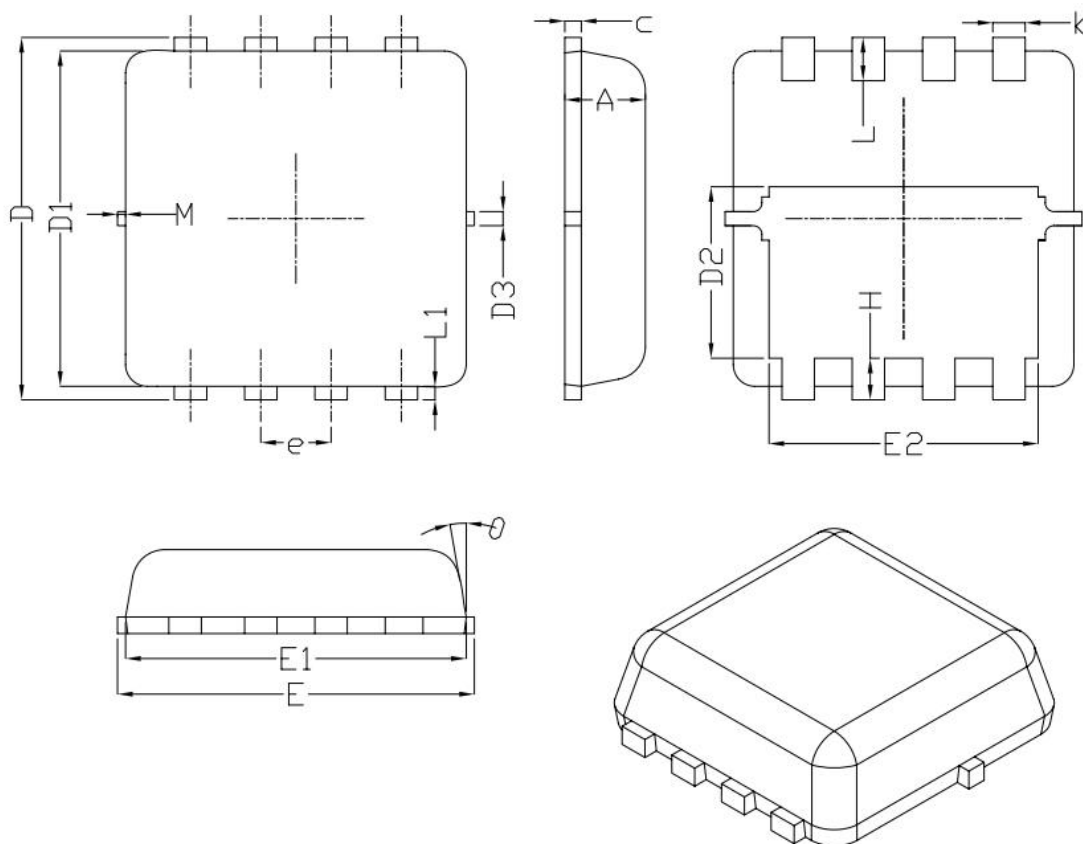


Figure 11 Normalized Maximum Transient Thermal Impedance

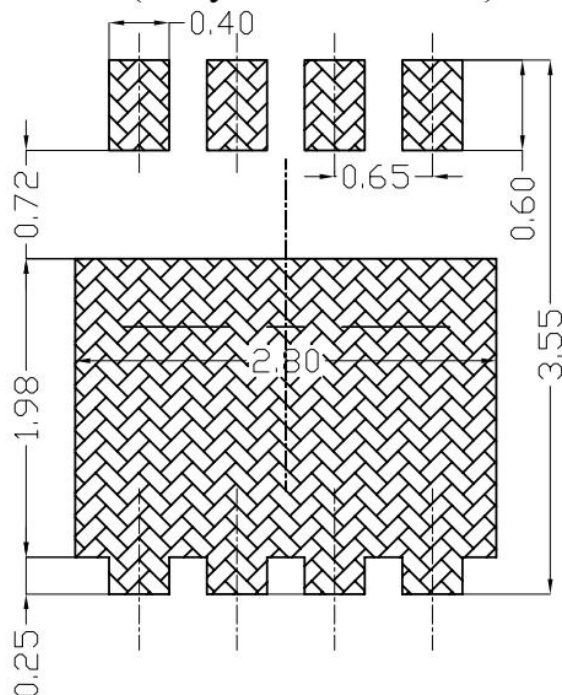
PDFN3.3X3.3-8L Package Information



SYMBOL	DIMENSIONAL REQMTS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
θ	---	10°	12°
M	*	*	0.15

* Not specified

Land Pattern (Only for Reference)



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