

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE30H10BK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

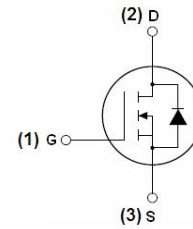
- $V_{DS} = 30V, I_D = 100A$
 $R_{DS(ON)} < 4.1m\Omega @ V_{GS} = 10V$ (Typ: 3.5m Ω)
 $R_{DS(ON)} < 7.0m\Omega @ V_{GS} = 4.5V$ (Typ: 5.8m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

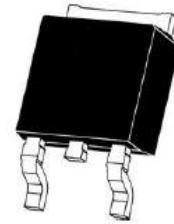
100% ΔV_{DS} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30H10BK	NCE30H10BK	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	70	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	110	W
Single pulse avalanche energy (Note 5)	E_{AS}	231	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	1.36	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

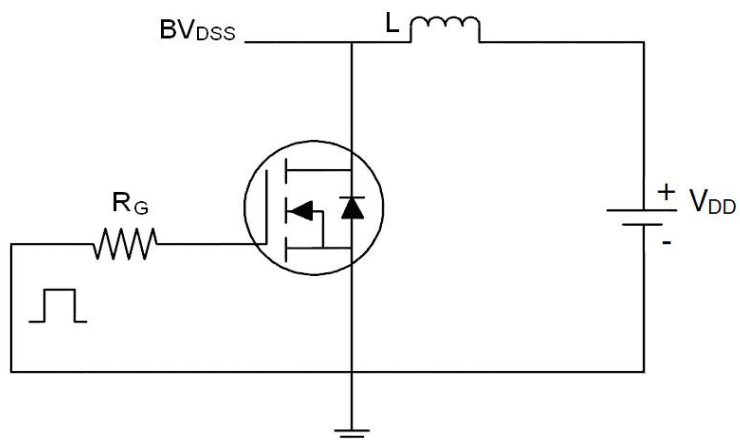
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.1	1.6	2.1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.5	4.1	mΩ
		V _{GS} =4.5V, I _D =20A	-	5.8	7.0	
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =20A	-	50	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, F=1.0MHz	-	2820	-	pF
Output Capacitance	C _{oss}		-	348	-	pF
Reverse Transfer Capacitance	C _{rss}		-	287	-	pF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =15V, I _D =20A V _{GS} =4.5V, R _{GEN} =1.8Ω	-	10.5	-	nS
Turn-on Rise Time	t _r		-	15	-	nS
Turn-Off Delay Time	t _{d(off)}		-	40	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =15V, I _D =20A, V _{GS} =10V	-	57.2	-	nC
Gate-Source Charge	Q _{gs}		-	7.5	-	nC
Gate-Drain Charge	Q _{gd}		-	12.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S	-	-	-	100	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 20A di/dt = 100A/μs ^(Note3)	-	55	-	nS
Reverse Recovery Charge	Q _{rr}		-	108	-	nC

Notes:

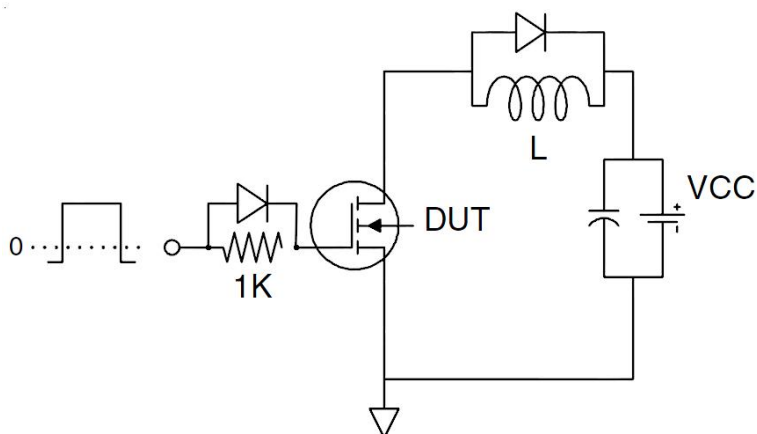
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=15V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test circuit

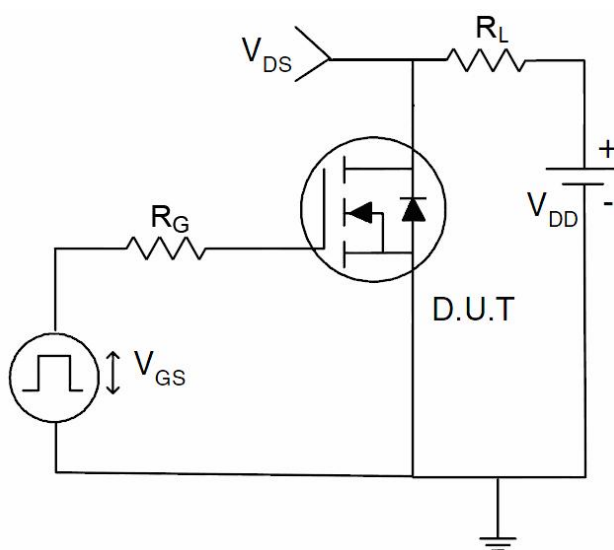
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

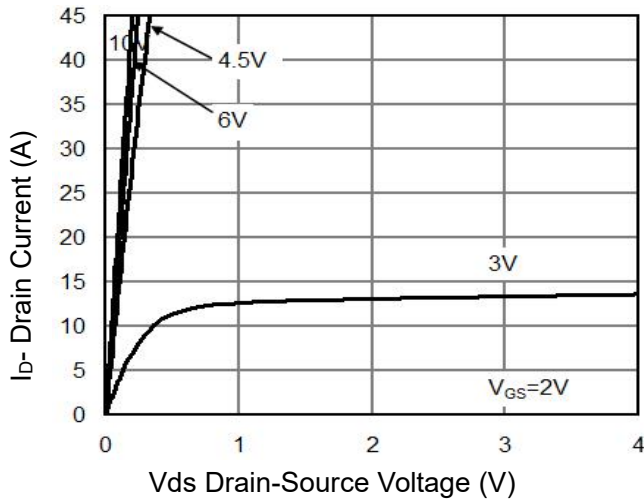


Figure 1 Output Characteristics

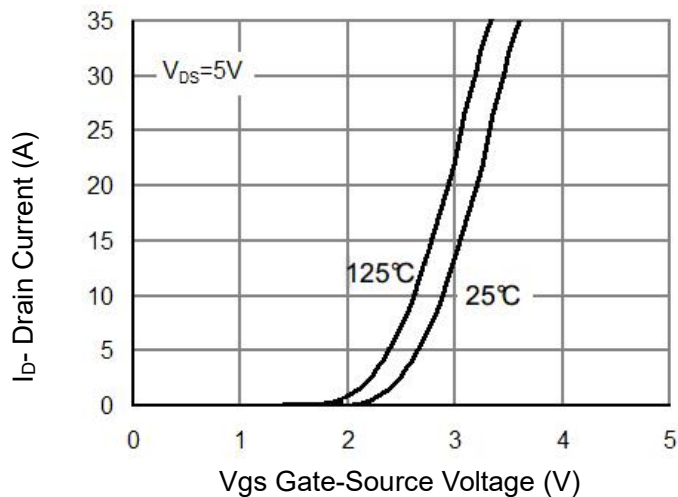


Figure 2 Transfer Characteristics

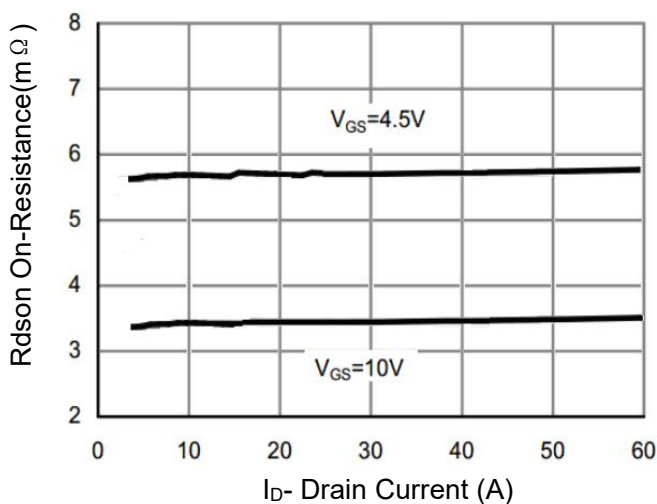


Figure 3 Rdson- Drain Current

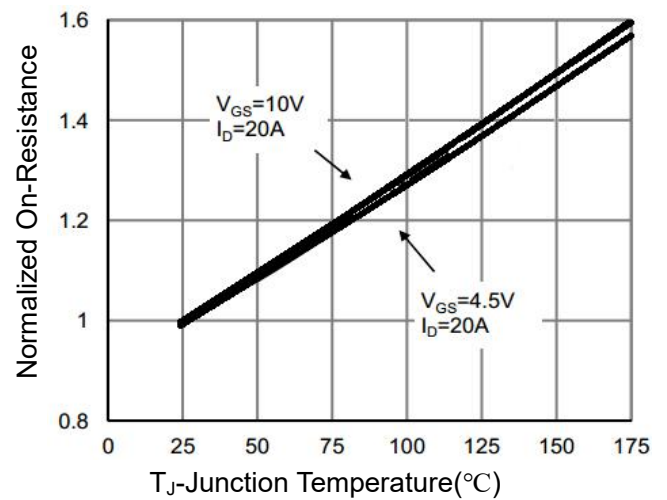


Figure 4 Rdson-Junction Temperature

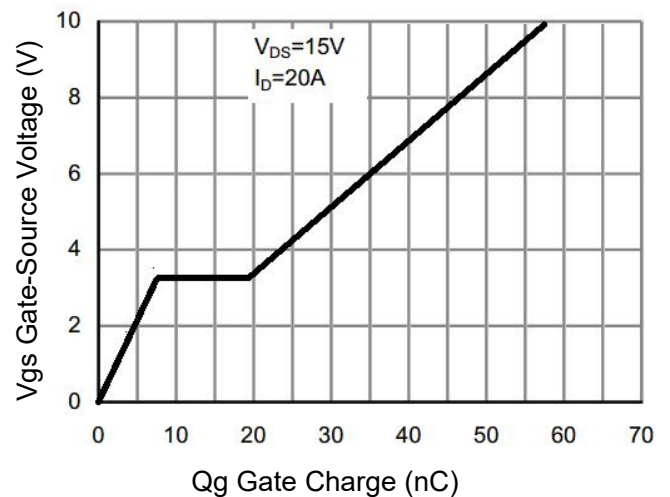


Figure 5 Gate Charge

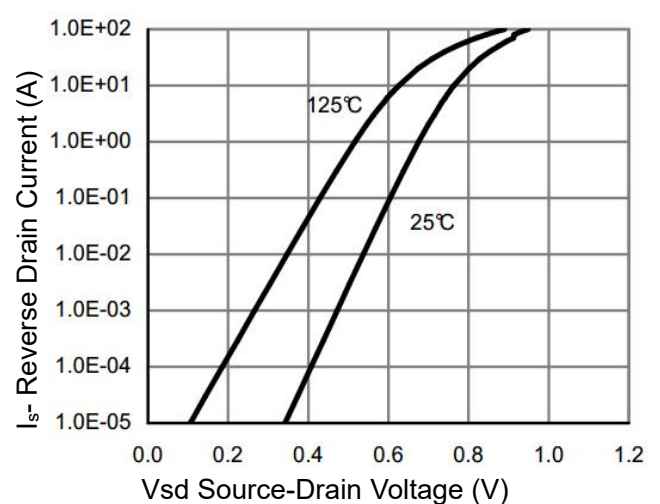


Figure 6 Source- Drain Diode Forward

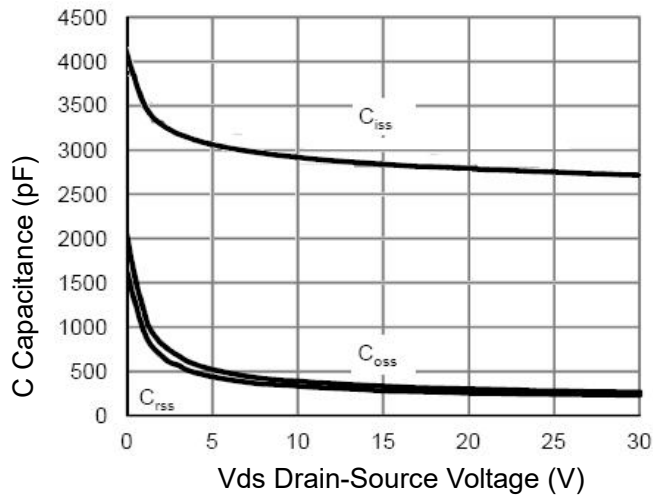


Figure 7 Capacitance vs Vds

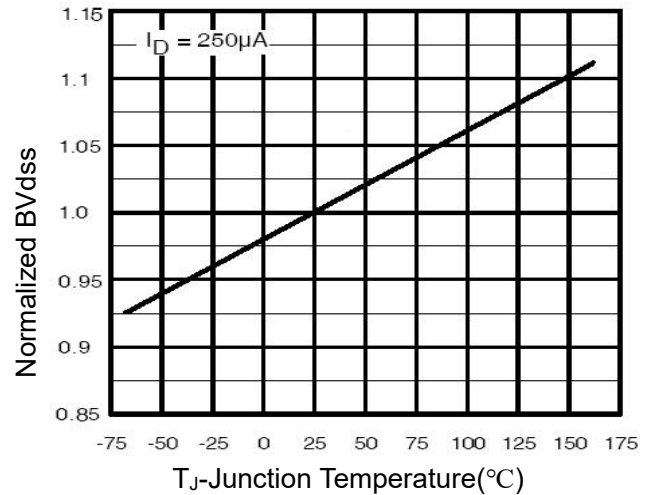


Figure 9 BV_{DSS} vs Junction Temperature

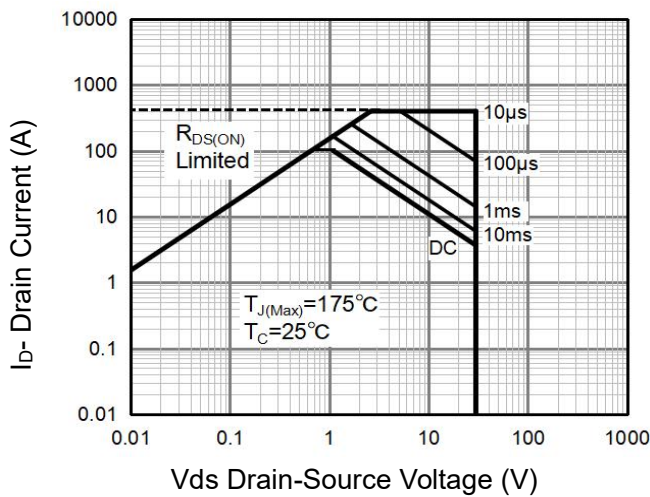


Figure 8 Safe Operation Area

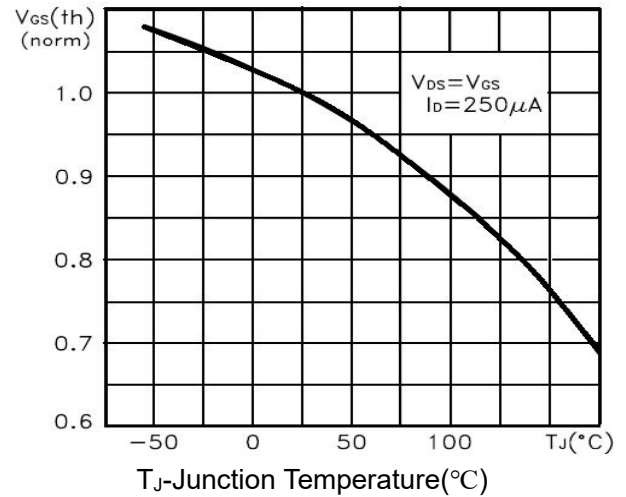


Figure 10 V_{GS(th)} vs Junction Temperature

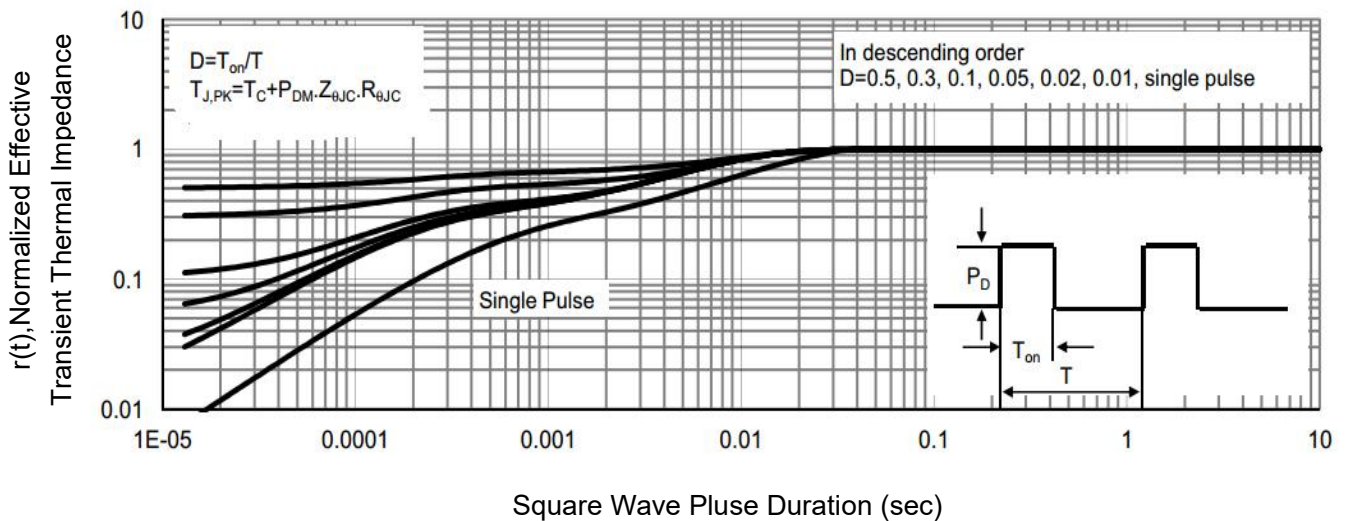
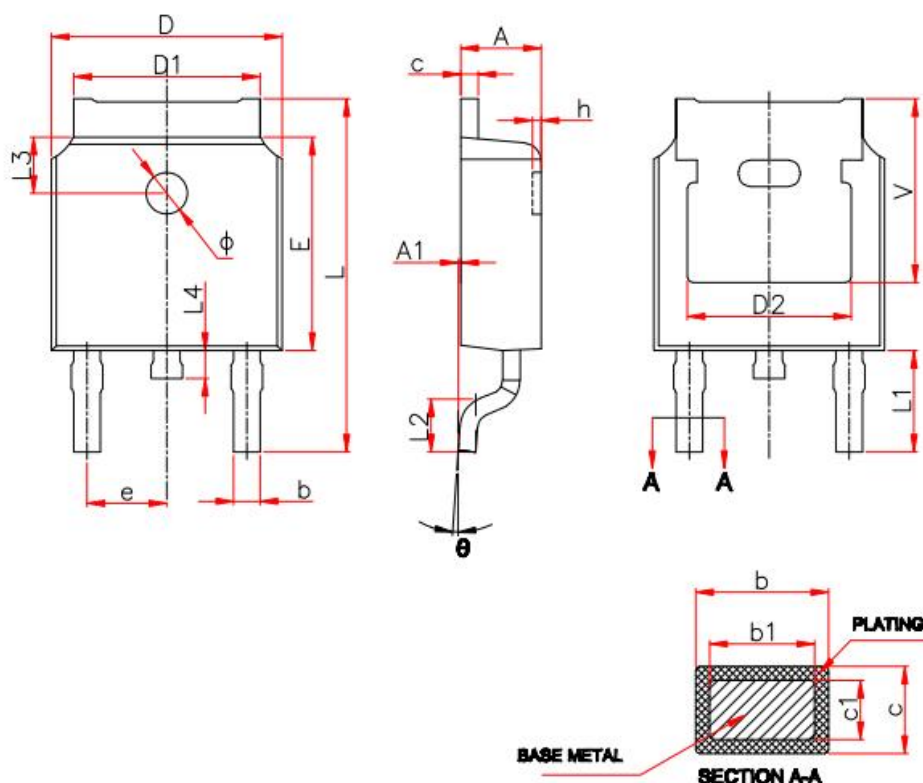


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
ϕ	1.10	1.30
θ	0°	8°

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