NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE30H12AK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

V_{DS} =30V,I_D =120A

 $R_{DS(ON)}$ <2.7m Ω @ V_{GS} =10V

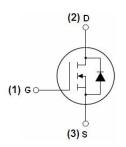
 $R_{DS(ON)}$ <3.8m Ω @ V_{GS} =4.5V

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED! 100% ΔVds TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30H12AK	NCE30H12AK	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	30	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	120	А
Drain Current-Continuous(Tc=100°C)	I _D (100℃)	84	Α
Pulsed Drain Current	I _{DM}	480	Α
Maximum Power Dissipation	P _D	120	W
Single pulse avalanche energy (Note 5)	E _{AS}	540	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	$^{\circ}$ C

Thermal Characteristic

Thermal Resistance,Junction-to-Case ^(Note 2)	R _{θJC}	1.25	°C/W
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Electrical Characteristics (T_A=25°C unless otherwise noted)

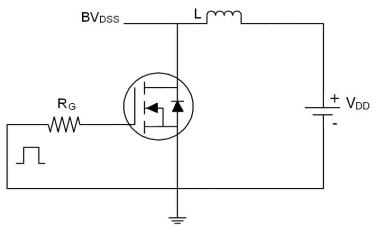
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics	•					
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)	•					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	0.7	1.1	1.4	V
Dunin Course On Otata Basistana		V _{GS} =10V, I _D =20A	-	2.1	2.7	mΩ
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =4.5V, I _D =15A	-	2.9	3.8	mΩ
Gate resistance	Rg	F=1.0MHz	-	1.2	-	Ω
Forward Transconductance	G FS	V _{DS} =10V,I _D =20A	50	-	-	S
Dynamic Characteristics (Note4)			1			
Input Capacitance	Clss	45)/)/ 0)/		3250		PF
Output Capacitance	Coss	$V_{DS}=15V, V_{GS}=0V,$		572		PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz		454		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}		-	11	-	nS
Turn-on Rise Time	t _r	V _{GS} =10V,V _{DS} =20V	-	10	-	nS
Turn-Off Delay Time	t _{d(off)}	$R_L=0.75\Omega, R_{GEN}=3\Omega$	-	38	-	nS
Turn-Off Fall Time	t _f		-	11	-	nS
Total Gate Charge	Qg			74		nC
Gate-Source Charge	Q _{gs}	V _{GS} =10V,V _{DS} =15V,I _D =15A		5.4		nC
Gate-Drain Charge	Q_{gd}	1		17.6		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =20A	-	-	1.2	V
Diode Forward Current (Note 2)	Is	-		-	120	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, I _F =20A	-	58	-	nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	115	-	nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LI				

Notes:

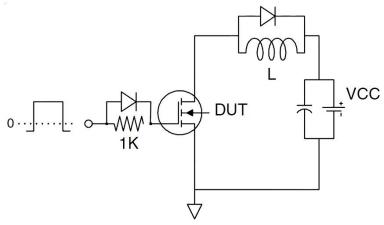
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}\text{C}$,VDD=15V,VG=10V,L=0.5mH,Rg=25 Ω

Test circuit

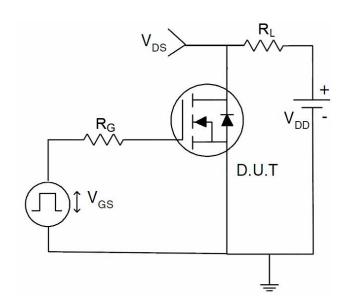
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

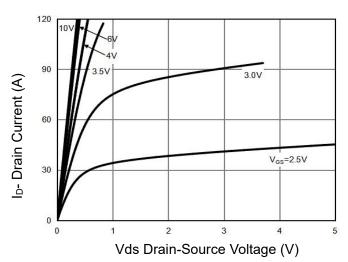


Figure 1 Output Characteristics

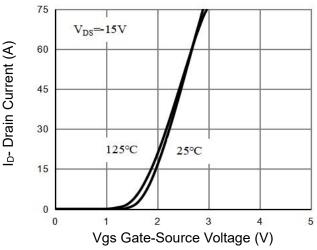


Figure 2 Transfer Characteristics

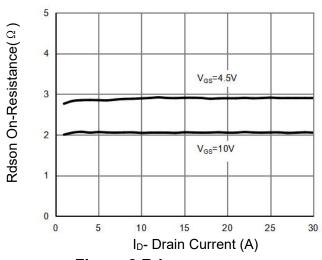


Figure 3 Rdson- Drain Current

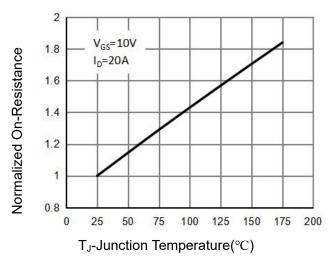


Figure 4 Rdson-Junction Temperature

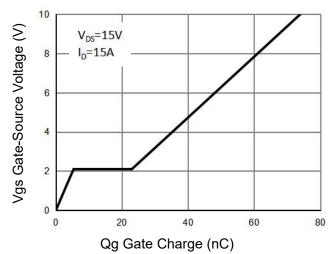


Figure 5 Gate Charge

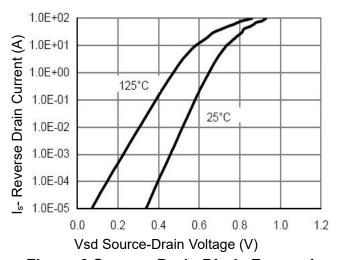


Figure 6 Source- Drain Diode Forward



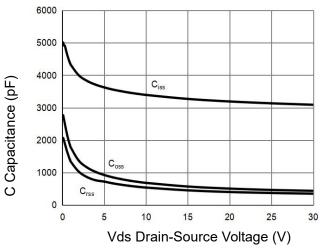


Figure 7 Capacitance vs Vds

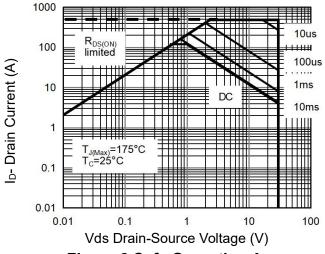


Figure 8 Safe Operation Area

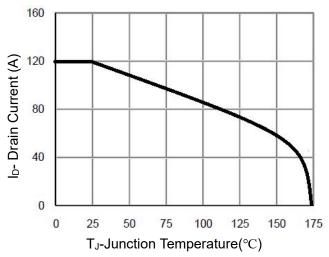


Figure 9 Current De-rating

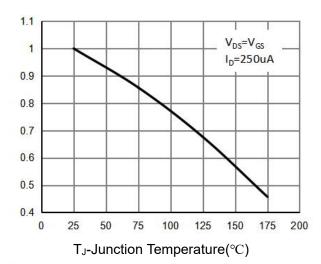


Figure 10 V_{GS(th)} vs Junction Temperature

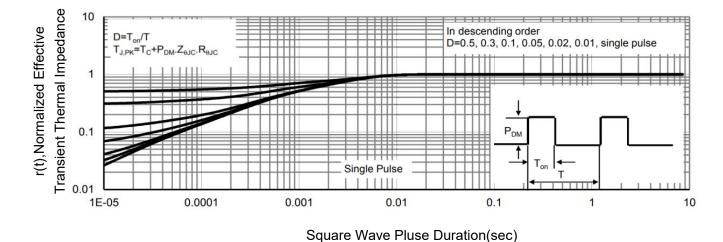
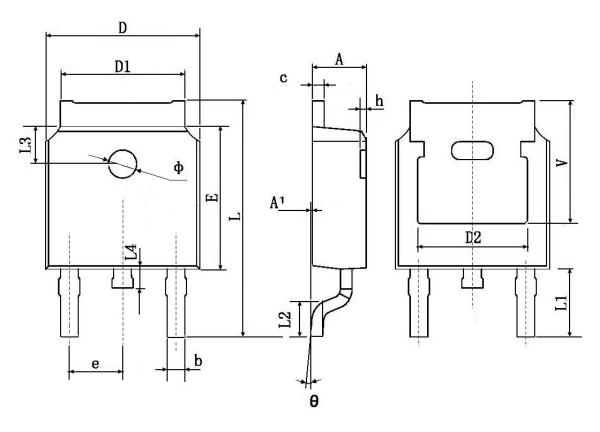


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Comphal	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.660	0.860	0.026	0.034	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	4.83	TYP.	0.190	TYP.	
E	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.800	10.400	0.386	0.409	
L1	2.900	2.900 TYP.		TYP.	
L2	1.400	1.700	0.055	0.067	
L3	1.600 TYP.		0.063	TYP.	
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.350	TYP.	0.211 TYP.		





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