NCE P-Channel Enhancement Mode Power MOSFET

Description

The NCE30P85K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge .This device is well suited for high current load applications.

General Features

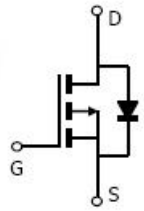
- V_{DS} = -30V,I_D = -85A
  $R_{DS(ON)}$ =5.3mΩ @ V_{GS}= -10V (Typ)
  $R_{DS(ON)}$ =7.6mΩ @ V_{GS}= -4.5V (Typ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

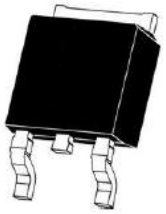
100% UIS TESTED!

100% ΔVds TESTED!



Schematic diagram

Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE30P85K	NCE30P85K	TO-252-2L	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-85	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	-60	A
Pulsed Drain Current	I_{DM}	-340	A
Maximum Power Dissipation	P_D	130	W
Single pulse avalanche energy (Note 5)	E_{AS}	912	mJ
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃

Thermal Characteristic

Thermal Resistance,Junction-to-Case(Note 2)	$R_{\theta JC}$	1.15	℃/W

Electrical Characteristics (T_C=25℃unless otherwise noted)

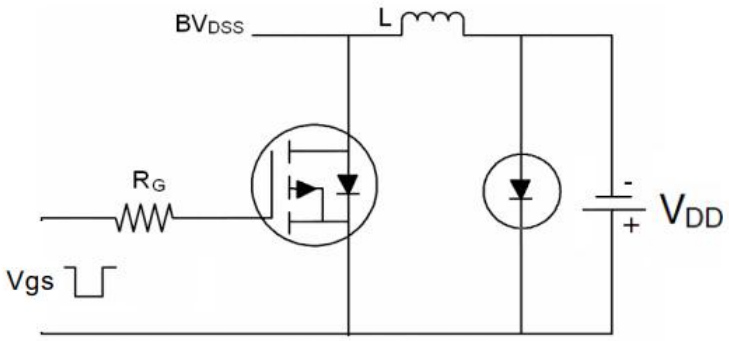
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D= -250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}= -30V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1.0	-1.6	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-20A	-	5.3	6.1	mΩ
		V_{GS}= -4.5V, I_D=-15A	-	7.6	10	mΩ
Forward Transconductance	g_{FS}	V_{DS}= -5V,I_D=-20A	-	60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	7016	-	PF
Output Capacitance	C_{oss}		-	838	-	PF
Reverse Transfer Capacitance	C_{rss}		-	616	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=-15V,I_D=-20A V_{GS}=-10V,R_G=3Ω	-	26	-	nS
Turn-on Rise Time	t_r		-	22	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	145	-	nS
Turn-Off Fall Time	t_f		-	70	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-20A, V_{GS}=-10V	-	92.5	-	nC
Gate-Source Charge	Q_{gs}		-	11.5	-	nC
Gate-Drain Charge	Q_{gd}		-	17	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-20A	-		-1.2	V
Diode Forward Current (Note 2)	I_S		-	-	-85	A
Reverse Recovery Time	t_{rr}	T_J = 25°C, I_F =- 20A di/dt = -100A/μs (Note3)	-	35		nS
Reverse Recovery Charge	Qrr		-	50		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

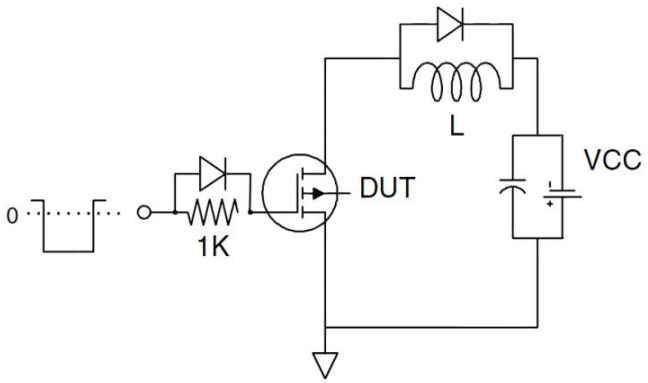
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board with 2oz. Copper, in a still air environment with T_A=25°C., t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-20V,V_G=-10V,L=0.5mH,Rg=25Ω

Test Circuit

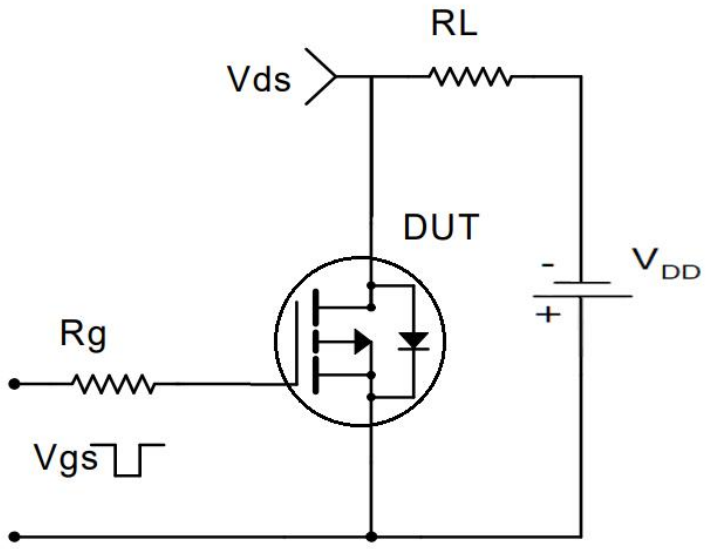
1）E_{AS} test Circuit



2）Gate charge test Circuit



3）Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

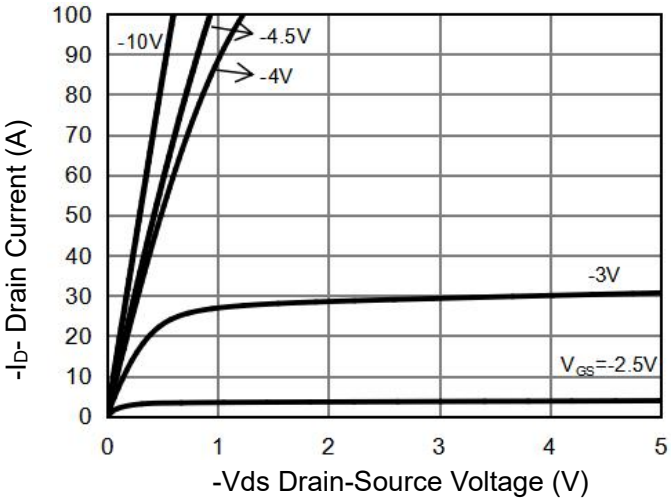


Figure 1 Output Characteristics

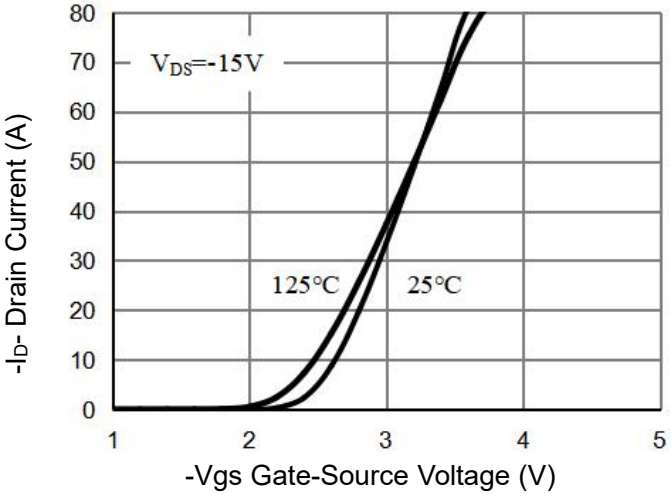


Figure 2 Transfer Characteristics

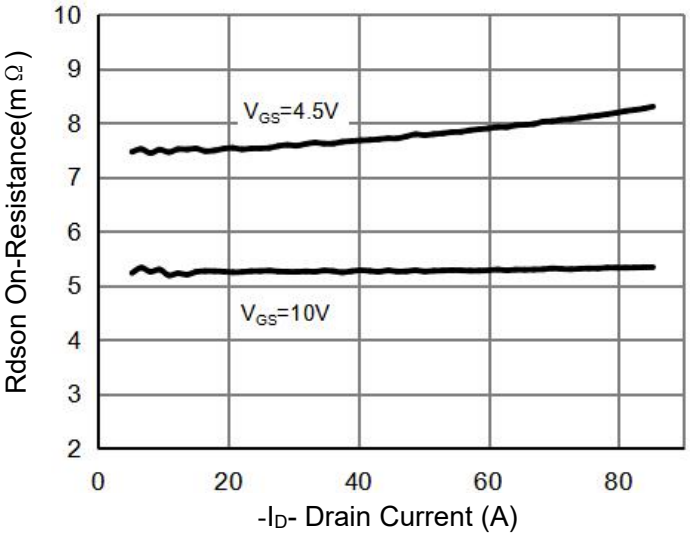


Figure 3 Rdson- Drain Current

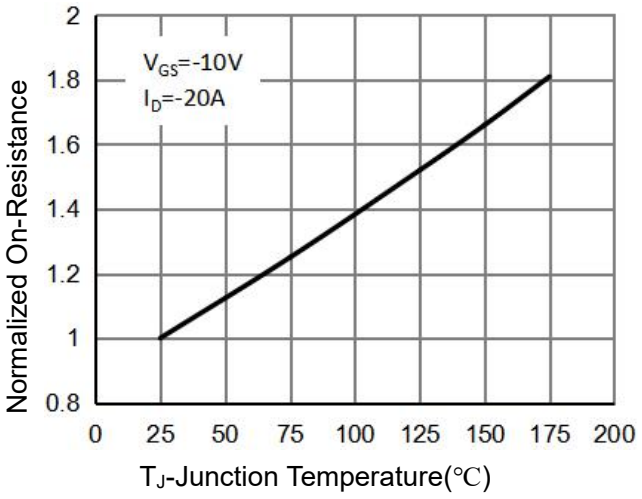


Figure 4 Rdson-Junction Temperature

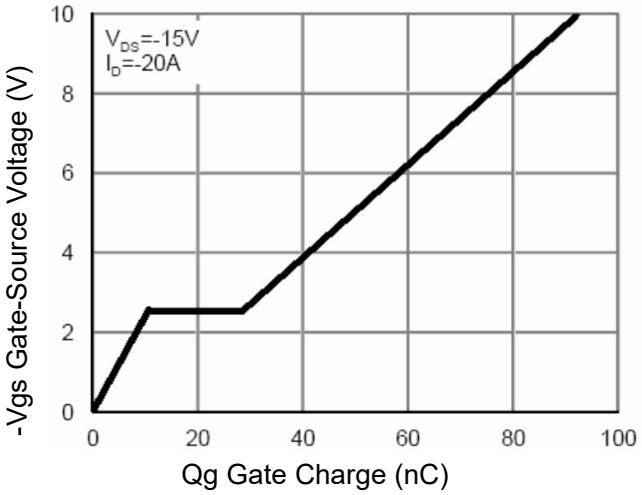


Figure 5 Gate Charge

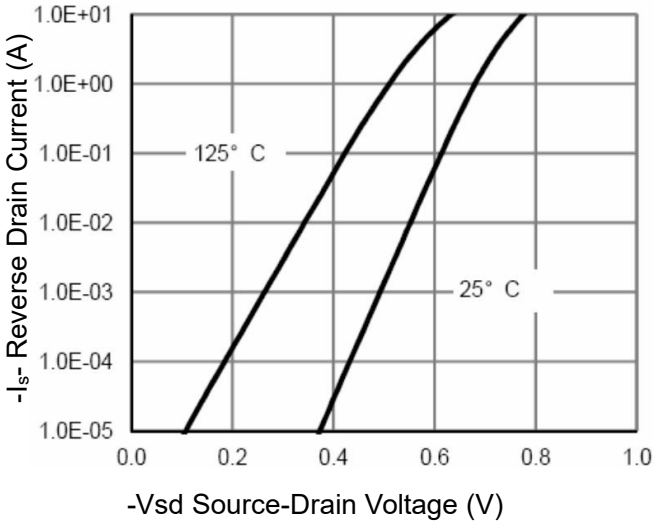


Figure 6 Source- Drain Diode Forward

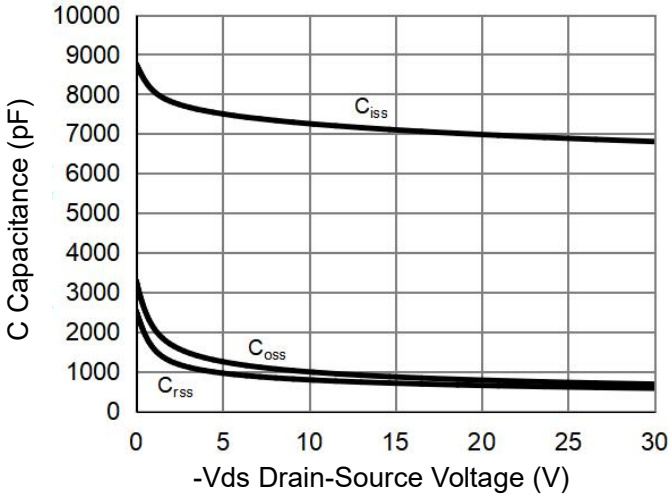


Figure 7 Capacitance vs Vds

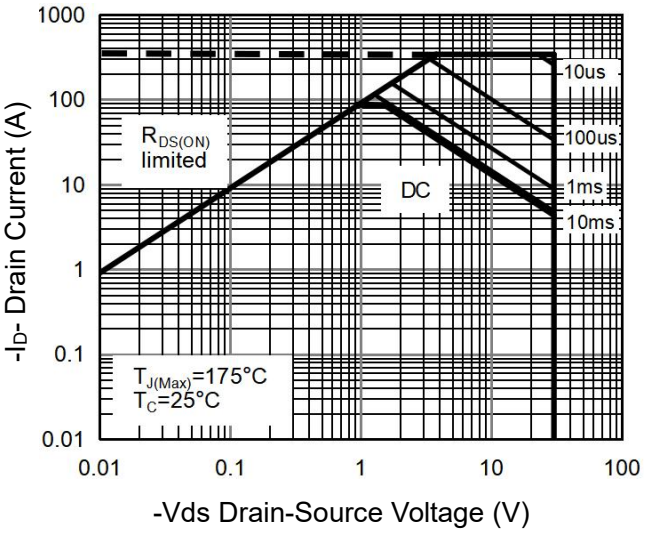


Figure 8 Safe Operation Area

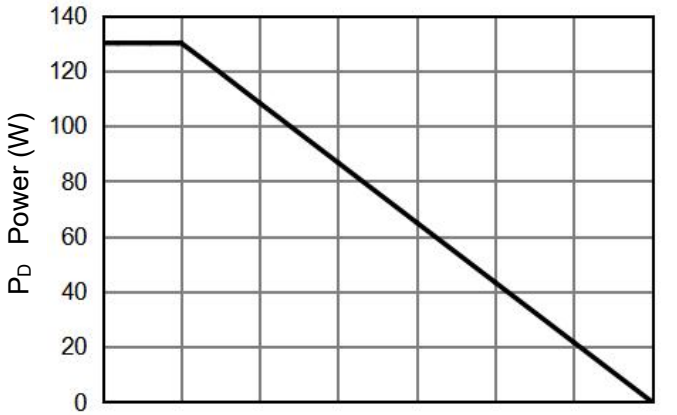


Figure 9 Power Dissipation

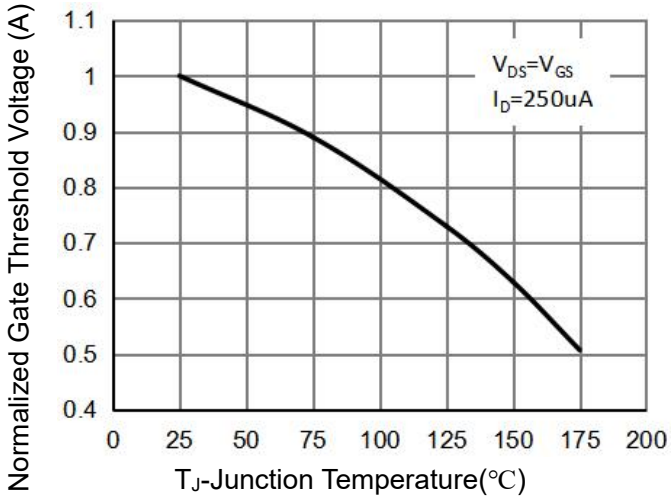


Figure 10 $V_{GS(th)}$ vs Junction Temperature

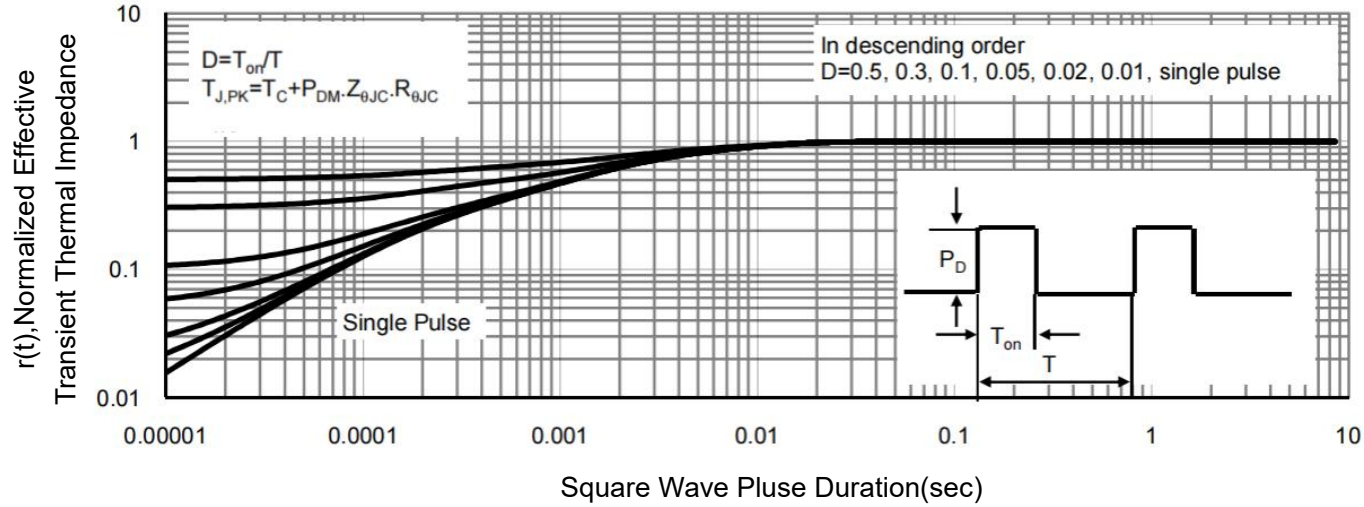
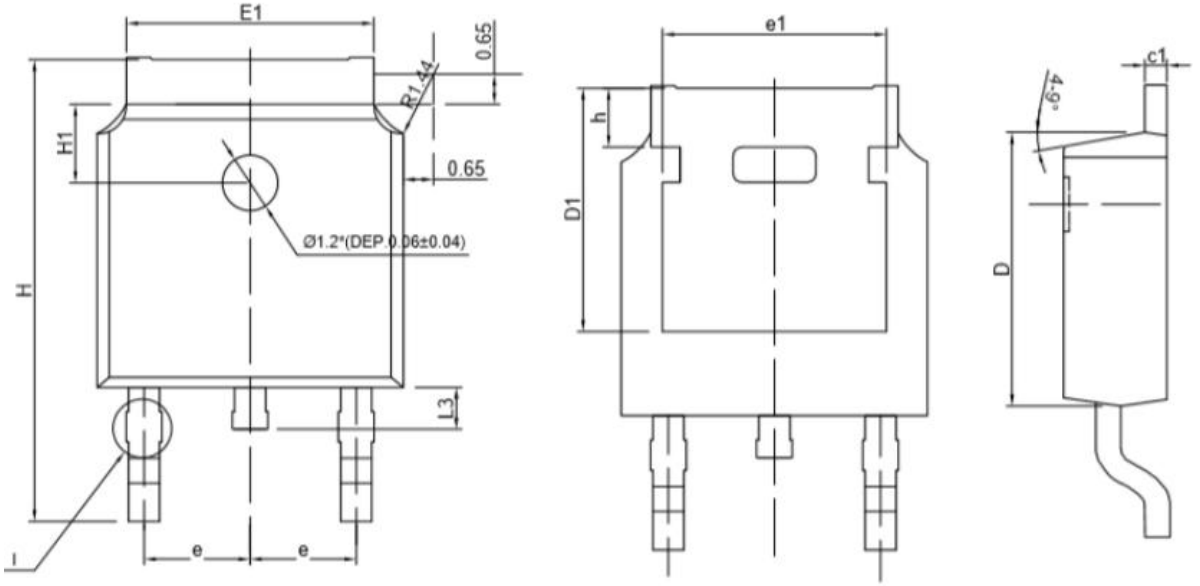
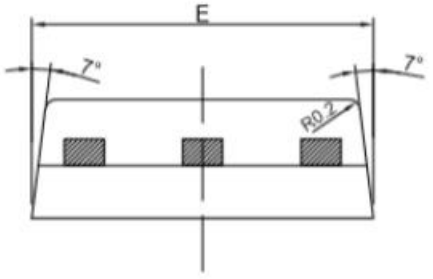
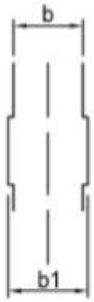


Figure 11 Normalized Maximum Transient Thermal Impedance

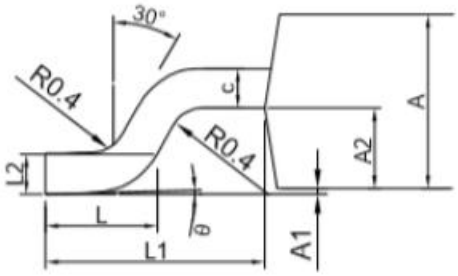
TO-252-2L Package Information







DETAIL I



SYMBOL	MIN	NOM	MAX
A	2.2	2.3	2.4
A1	0.00	0.075	0.15
A2	0.97	1.02	1.07
b	0.60	0.67	0.74
b1	0.65	-	1.15
c	0.508	0.528	0.548
c1	0.478	0.508	0.538
D	6.0	6.1	6.2
D1	5.15	5.25	5.35
E	6.5	6.6	6.7
E1	5.184	5.334	5.484
e		2.286BSC	
e1	4.806	4.826	4.846
H	9.8	10.0	10.2
H1	1.5	1.6	1.7
h	1.15	1.25	1.35
L	1.4	1.5	1.6
L1		2.888REF	
L2		0.51BSC	
L3	0.8	0.9	1.0
θ	0°	-	10°

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