

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE6058K uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

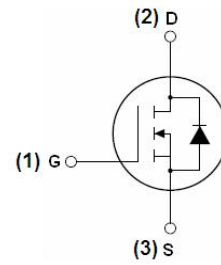
- $V_{DS} = 60V, I_D = 58A$
 $R_{DS(ON)} < 10m\Omega @ V_{GS} = 10V$ (Typ: 8.5m Ω)
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- LED backlighting
- Uninterruptible power supply

100% UIS TESTED!

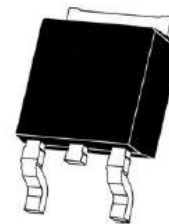
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE6058K	NCE6058K	TO-252-2L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	58	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	41	A
Pulsed Drain Current	I_{DM}	232	A
Maximum Power Dissipation	P_D	85	W
Debating factor		0.57	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	290	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	1.76	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_c=25^{\circ}\text{C}$ unless otherwise noted)

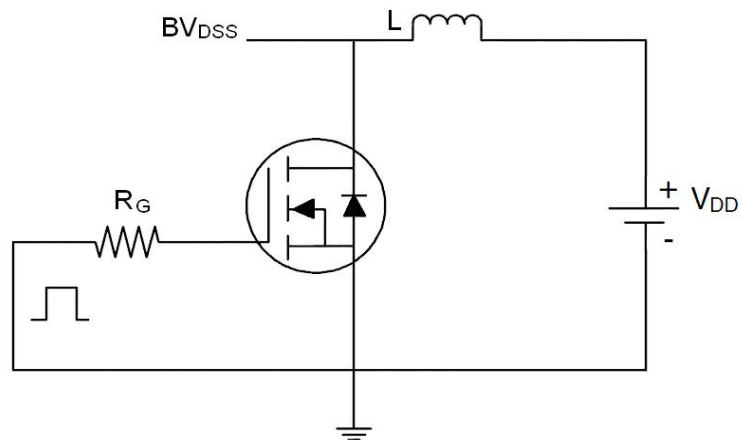
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =30A	-	8.5	10	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =30A	30	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V, F=1.0MHz	-	2970	-	PF
Output Capacitance	C _{oss}		-	181	-	PF
Reverse Transfer Capacitance	C _{rss}		-	161	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V,R _L =1Ω V _{GS} =10V,R _{GEN} =3Ω	-	12	-	nS
Turn-on Rise Time	t _r		-	5.2	-	nS
Turn-Off Delay Time	t _{d(off)}		-	38	-	nS
Turn-Off Fall Time	t _f		-	27	-	nS
Total Gate Charge	Q _g	V _{DS} =30V,I _D =30A, V _{GS} =10V	-	60	-	nC
Gate-Source Charge	Q _{gs}		-	14.6	-	nC
Gate-Drain Charge	Q _{gd}		-	17	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V,I _S =30A	-	-	1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	58	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =30A di/dt = 100A/μs ^(Note3)	-	35		nS
Reverse Recovery Charge	Q _{rr}		-	47		nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

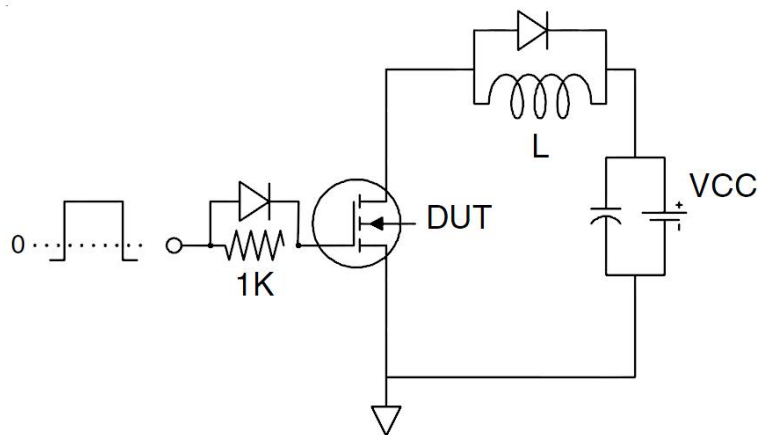
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test circuit

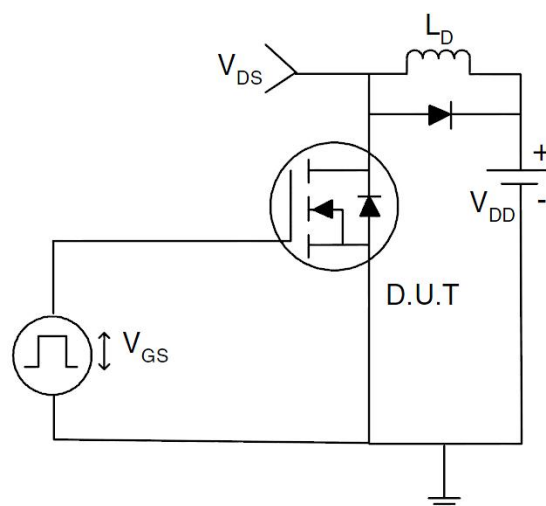
1) E_{AS} test Circuits



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

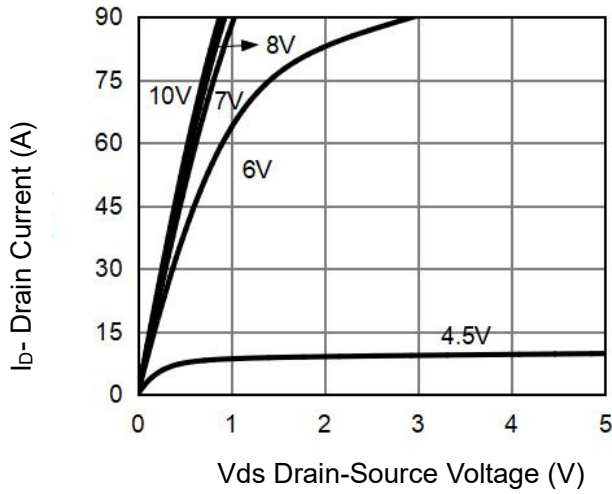


Figure 1 Output Characteristics

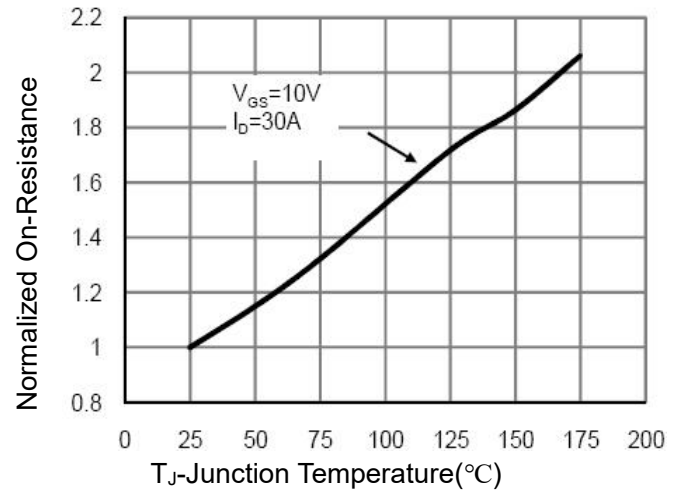


Figure 4 Rdson-Junction Temperature

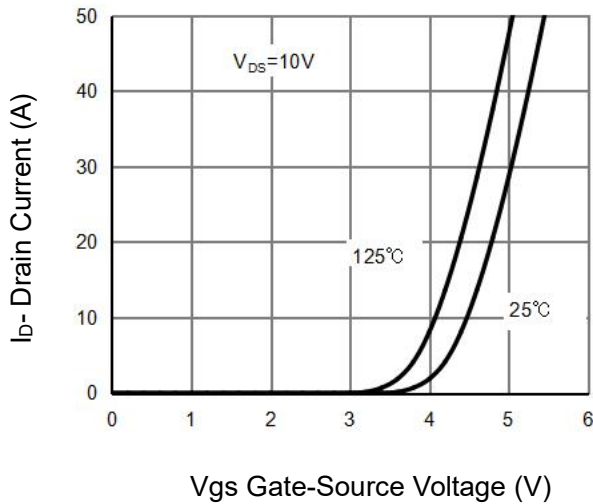


Figure 2 Transfer Characteristics

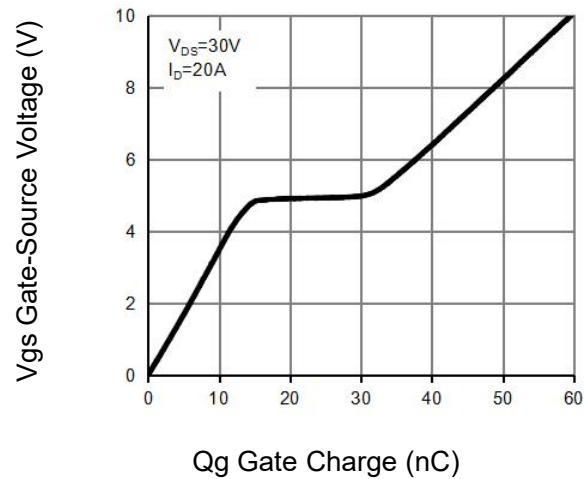


Figure 5 Gate Charge

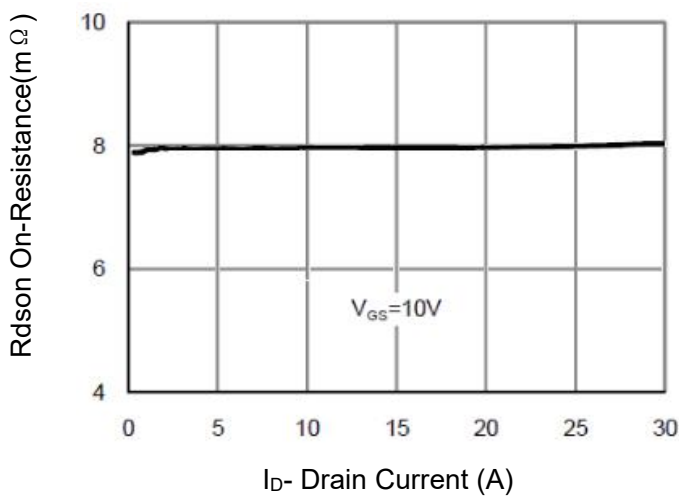


Figure 3 Rdson- Drain Current

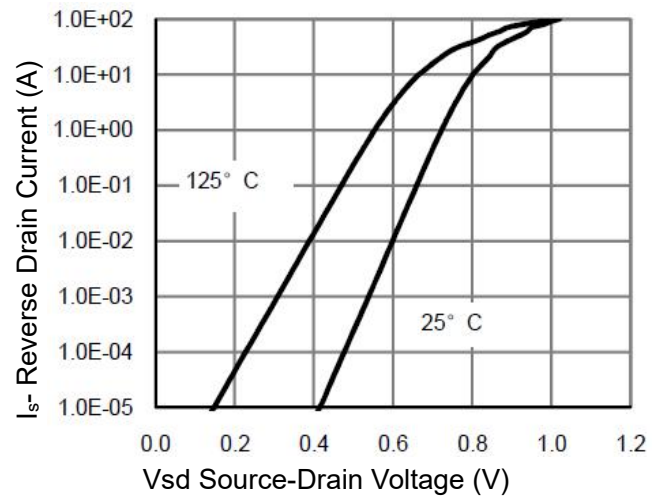


Figure 6 Source- Drain Diode Forward

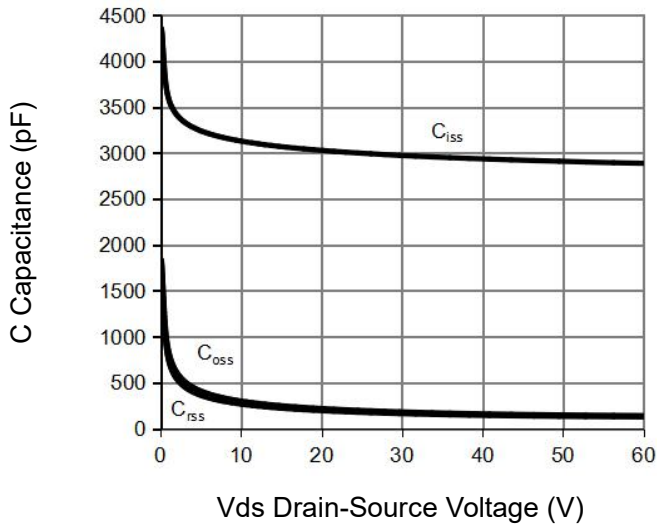


Figure 7 Capacitance vs Vds

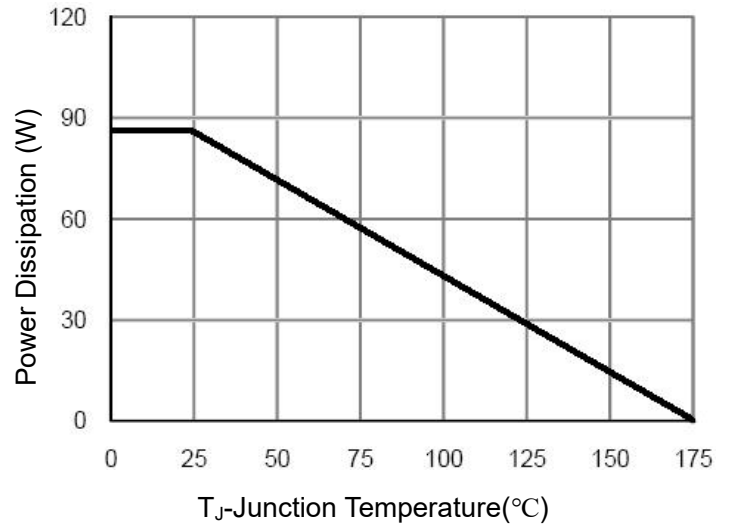


Figure 9 Power De-rating

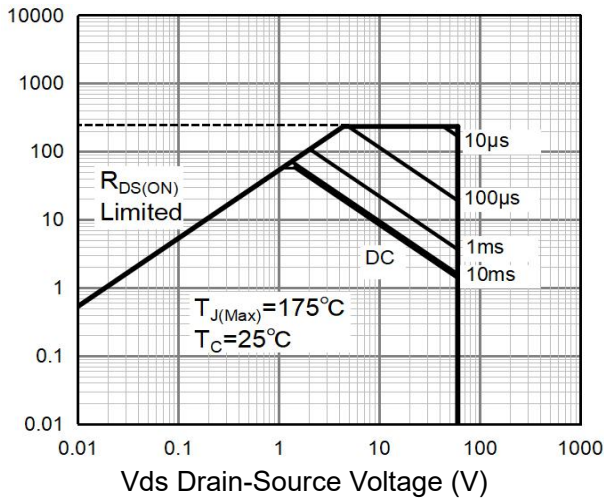


Figure 8 Safe Operation Area

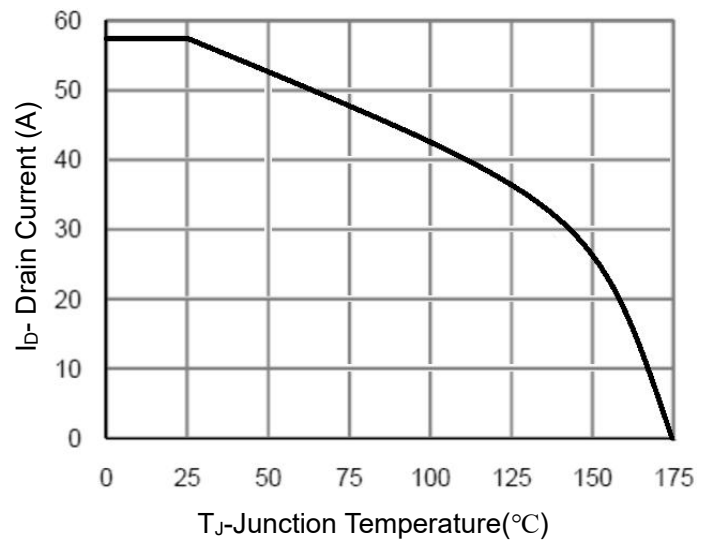


Figure 10 ID Current- Junction Temperature

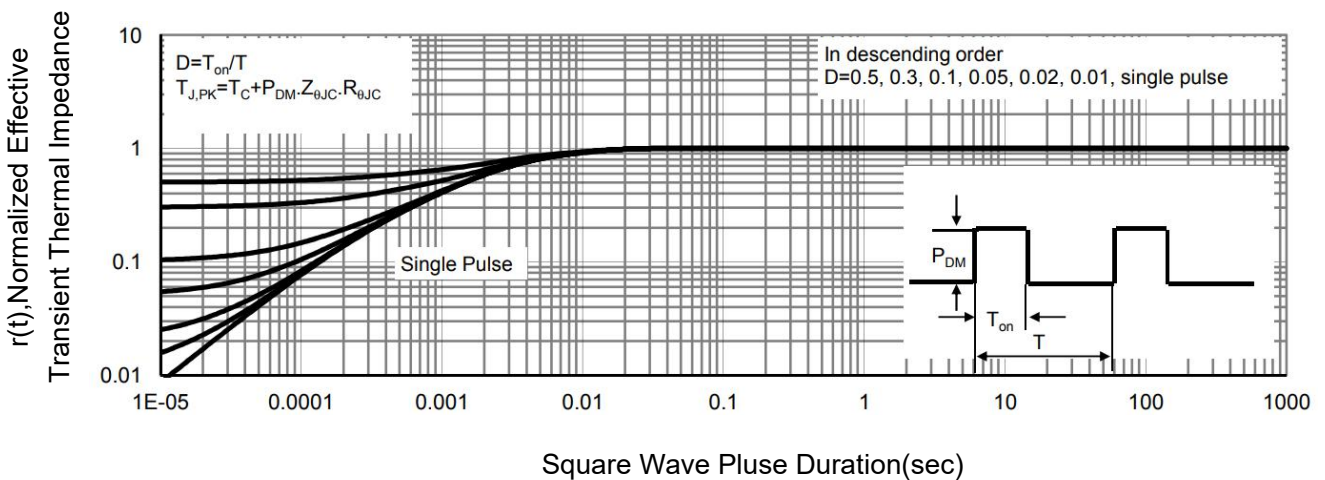
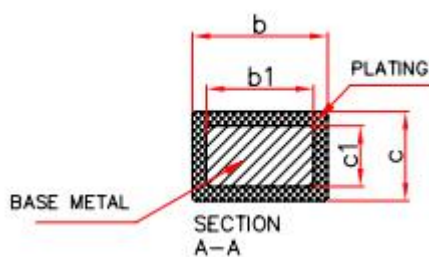
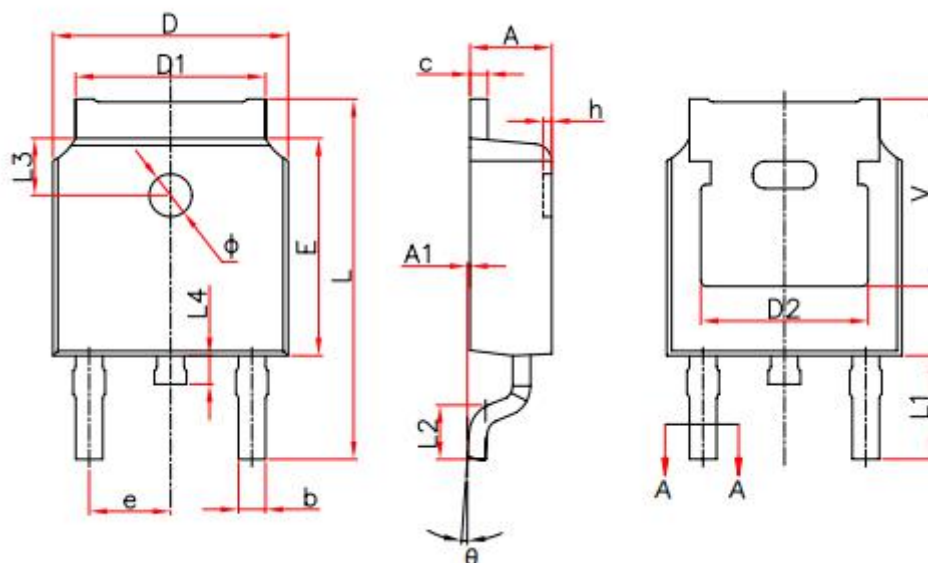


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
Φ	1.10	1.30
θ	0°	8°
h	0.00	0.30
V	5.35 REF.	

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