

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE6080EK uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

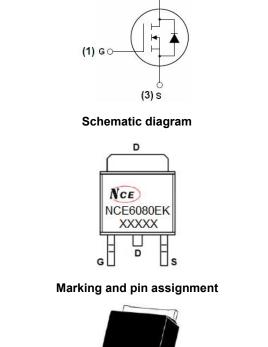
- V_{DS} =60V,I_D =80A
- R_{DS(ON)} <6.9mΩ @ V_{GS}=10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAs
- Excellent package for good heat dissipation

Application

- PWM
- Load Switching

100% UIS TESTED!

100% ΔVds TESTED!



(2) D



TO-252-2L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE6080EK	NCE6080EK	TO-252-2L	-	-	-

Absolute Maximum Ratings (Tc=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	Vds	60	V
Gate-Source Voltage	Vgs	±20	V
Drain Current-Continuous	Ι _D	80	A
Drain Current-Continuous(Tc=100℃)	l₀(100℃)	56.5	A
Pulsed Drain Current	I _{DM}	320	A
Maximum Power Dissipation	PD	110	W
Derating factor		0.73	W/℃
Single pulse avalanche energy (Note 5)	Eas	390	mJ
Operating Junction and Storage Temperature Range	T _J ,T _{STG}	-55 To 175	°C



Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	R _{θJC}	1.36	°C /W
Thermal Resistance, Junction-to-Ambient ^(Note 2)	R _{0JA}	60	°C /W

Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	neter Symbol Condition		Min	Тур	Max	Unit	
Off Characteristics			-				
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	60	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA	
Gate-Body Leakage Current	lgss	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA	
On Characteristics (Note 3)							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250µA	2	2.8	4	V	
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	6	6.9	mΩ	
Forward Transconductance	G FS	V _{DS} =5V,I _D =20A	20	-	-	S	
Dynamic Characteristics (Note4)	ł	L					
Input Capacitance	Clss	<u>)</u>	-	4000	-	PF	
Output Capacitance	Coss	V_{DS} =30V, V_{GS} =0V,	-	290	-	PF	
Reverse Transfer Capacitance	C _{rss}	F=1.0MHz	-	210	-	PF	
Switching Characteristics (Note 4)	I						
Turn-on Delay Time	t _{d(on)}		-	8.5	-	nS	
Turn-on Rise Time	tr	V _{DD} =30V,R∟=1Ω	-	7	-	nS	
Turn-Off Delay Time	t _{d(off)}	V _{GS} =10V,R _G =3Ω	-	40	-	nS	
Turn-Off Fall Time	t _f		-	15	-	nS	
Total Gate Charge	Qg	N/ 001/1 001	-	90		nC	
Gate-Source Charge	Q _{gs}	V_{DS} =30V,I _D =20A,	-	9		nC	
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	18		nC	
Drain-Source Diode Characteristics			-				
Diode Forward Voltage (Note 3)	Vsd	V _{GS} =0V,I _S =20A	-		1.2	V	
Diode Forward Current (Note 2)	Is		-	-	80	A	
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 20A	-	32	-	nS	
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	45	-	nC	
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD					

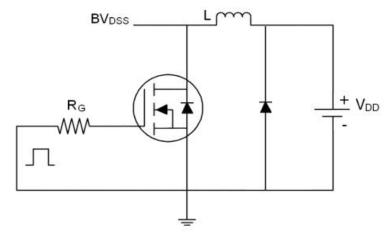
Notes:

- **1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width \leq 300µs, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- **5.** E_{AS} condition : Tj=25 $^\circ C$,V_DD=20V,V_G=10V,L=0.5mH,Rg=25\Omega

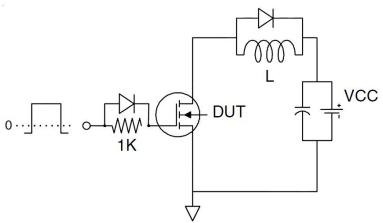


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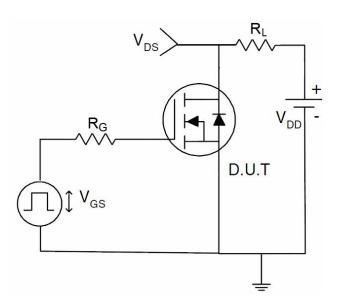
Test circuit 1) E_{AS} Test Circuit



2) Gate Charge Test Circuit

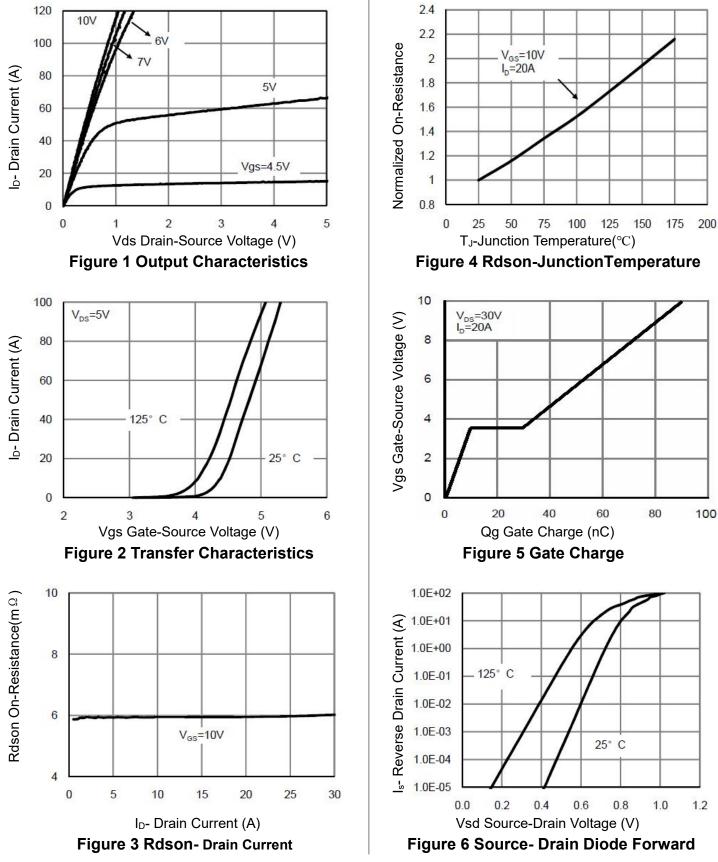


3) Switch Time Test Circuit



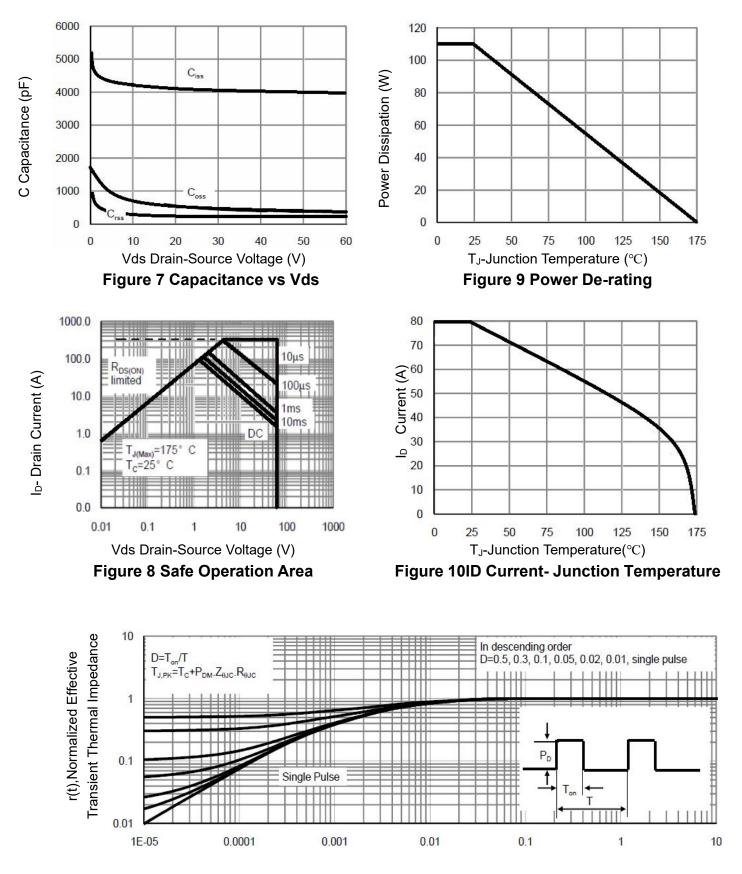








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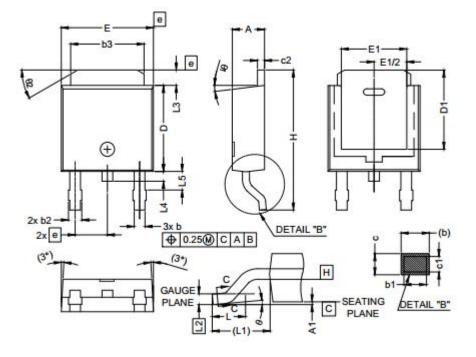


Square Wave Pluse Duration(sec)

Figure 11 Normalized Maximum Transient Thermal Impedance



TO-252-2L Package Information



SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.	SYMBOL	MIN.	MAX.
A	2.18	2.39	E	6.35	6.73	θ1	0°	15°
A1	-	0.13	E1	4.32	Ξ	θ2	25°	35°
b	0.65	0.89	е	2.29 BSC				
b1	0.64	0.79	Н	9.94	10.34			
b2	0.76	1.13	L	1.50	1.78			
b3	4.95	5.46	L1	2.74	REF			
С	0.46	0.61	L2	0.51 BSC				
c1	0.41	0.56	L3	0.89	1.27			
c2	0.46	0.60	L4	-	1.02			
D	5.97	6.22	L5	1.14	1.49			
D1	5.21		θ	0°	10°			



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