

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE60H10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

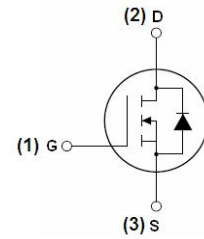
- $V_{DS} = 60V, I_D = 100A$
 $R_{DS(ON)} < 5.2m\Omega @ V_{GS}=10V$ (Typ:4.5m Ω)
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

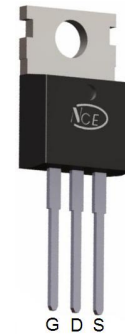
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE60H10	NCE60H10	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	100	A
Drain Current-Continuous($T_C=100^\circ C$)	$I_D(100^\circ C)$	70	A
Pulsed Drain Current	I_{DM}	400	A
Maximum Power Dissipation	P_D	170	W
Derating factor		1.13	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	812	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.88	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

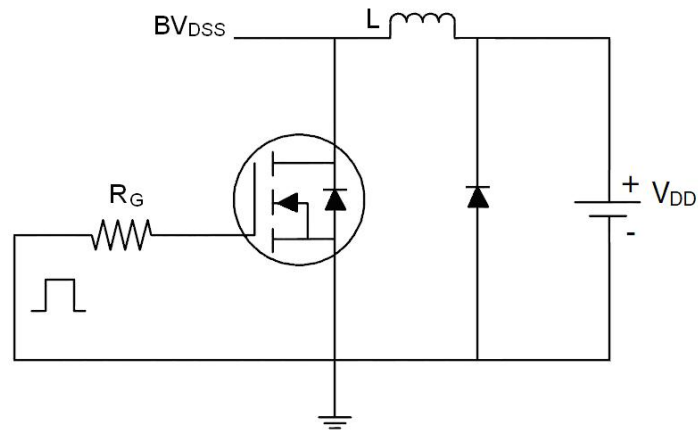
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	4.5	5.2	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	50	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	5200	-	PF
Output Capacitance	C _{oss}		-	410	-	PF
Reverse Transfer Capacitance	C _{rss}		-	330	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	VDD=30V, RL=1.5Ω RG=2.5Ω, VGS=10V	-	17	-	nS
Turn-on Rise Time	t _r		-	11	-	nS
Turn-Off Delay Time	t _{d(off)}		-	55	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =20A, V _{GS} =10V	-	100	-	nC
Gate-Source Charge	Q _{gs}		-	21	-	nC
Gate-Drain Charge	Q _{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	100	A
Reverse Recovery Time	t _{rr}	T _J =25℃, I _F =100A di/dt=100A/μs <small>(Note3)</small>	-		37	nS
Reverse Recovery Charge	Q _{rr}		-		58	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

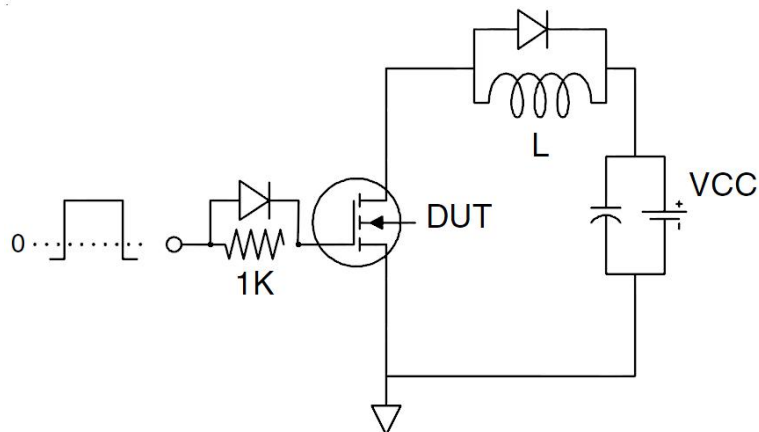
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=35V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

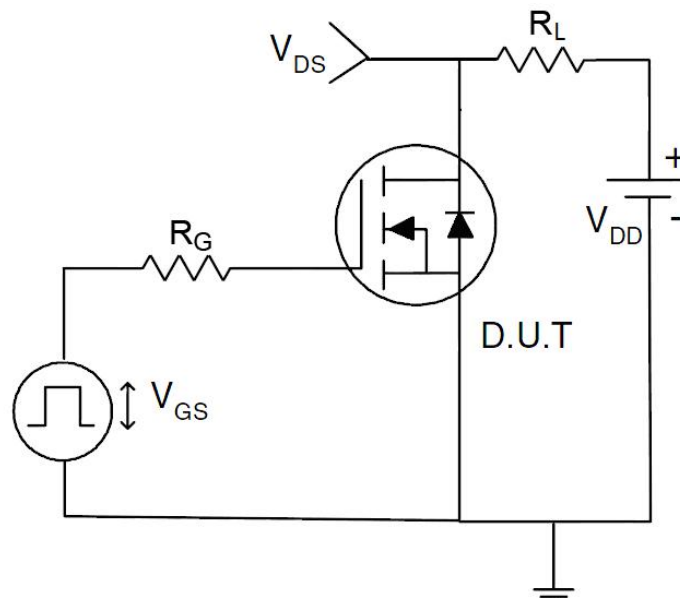
1) EAS Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

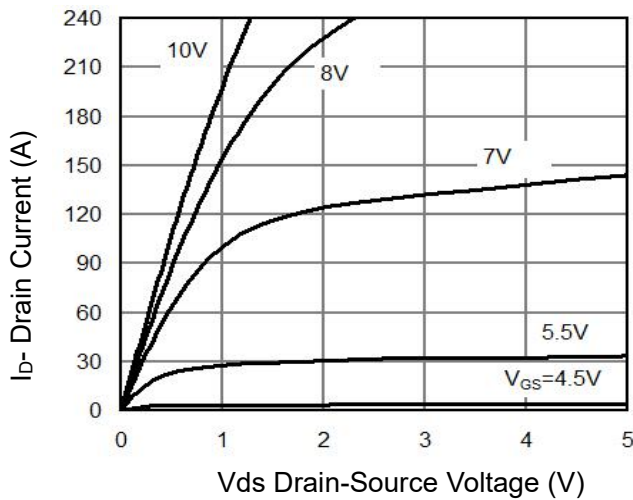


Figure 1 Output Characteristics

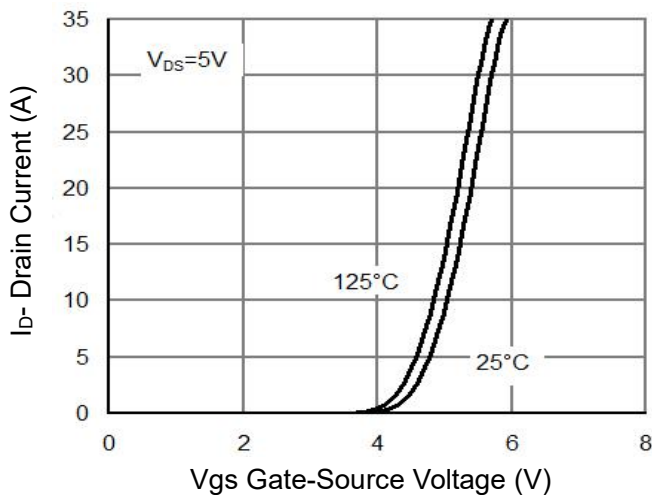


Figure 2 Transfer Characteristics

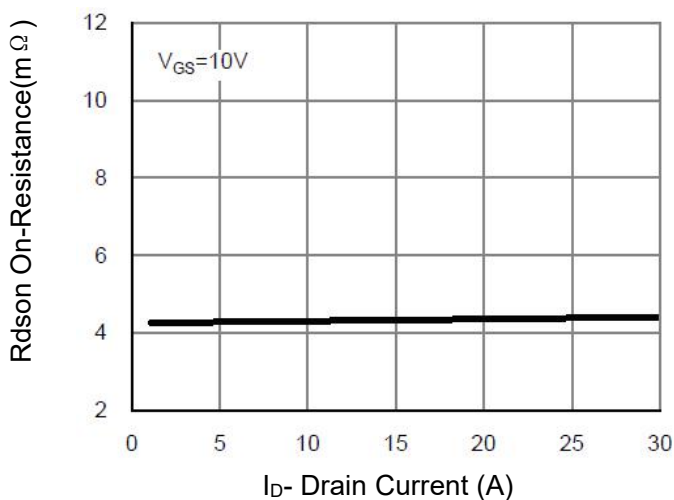


Figure 3 $R_{DS(on)}$ - Drain Current

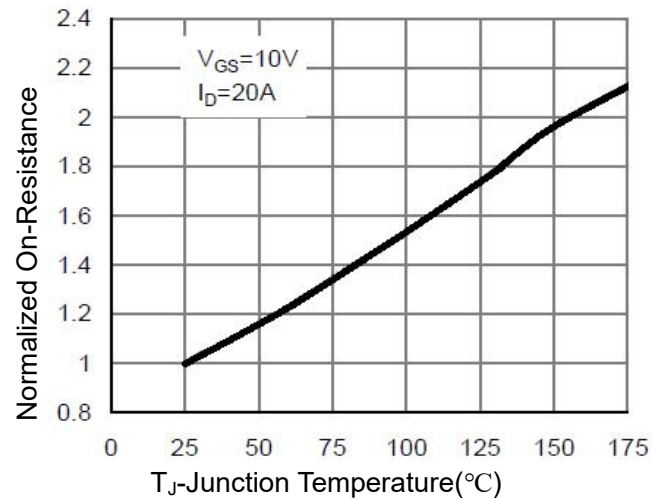


Figure 4 $R_{DS(on)}$ -Junction Temperature

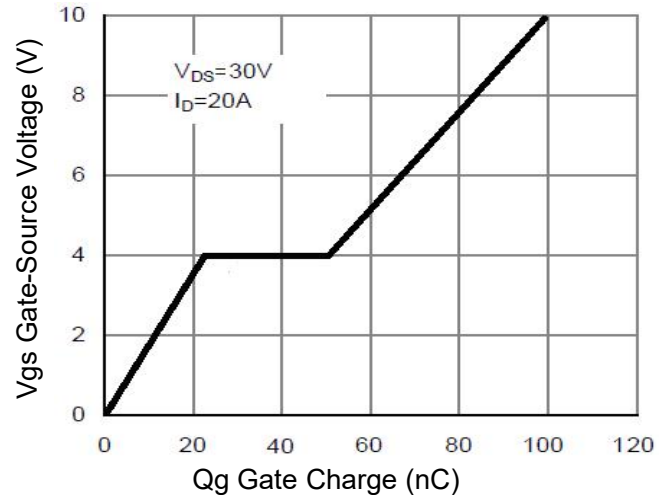


Figure 5 Gate Charge

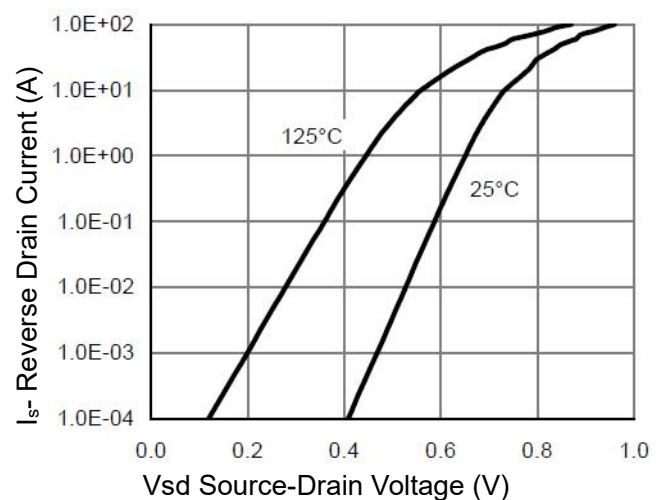


Figure 6 Source- Drain Diode Forward

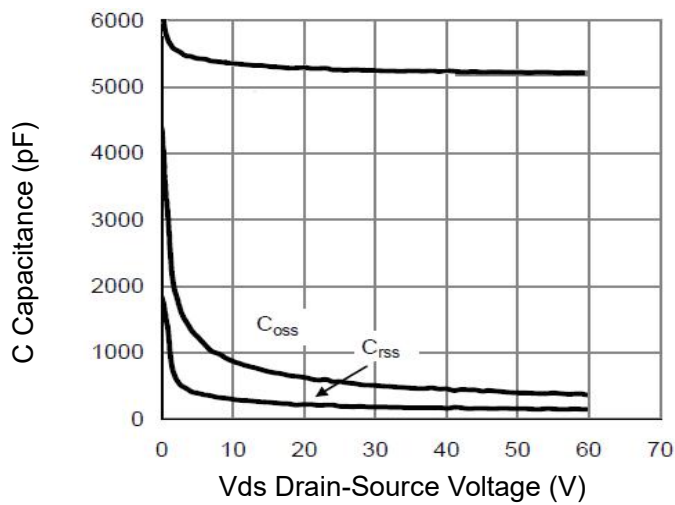


Figure 7 Capacitance vs Vds

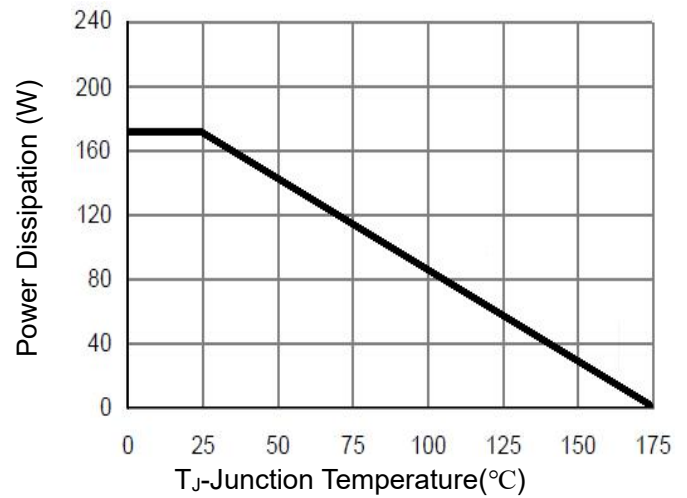


Figure 9 Power De-rating

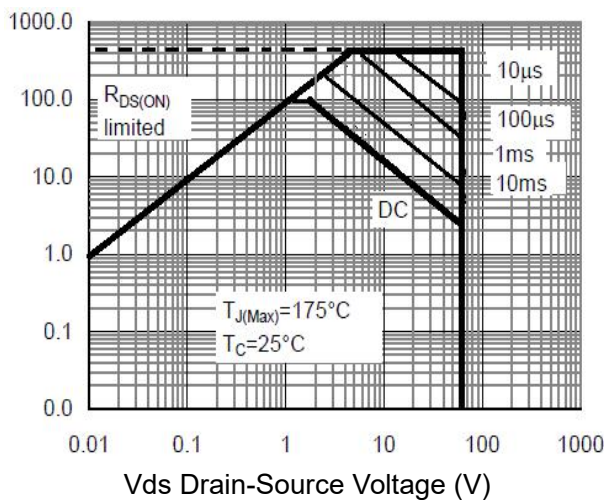


Figure 8 Safe Operation Area

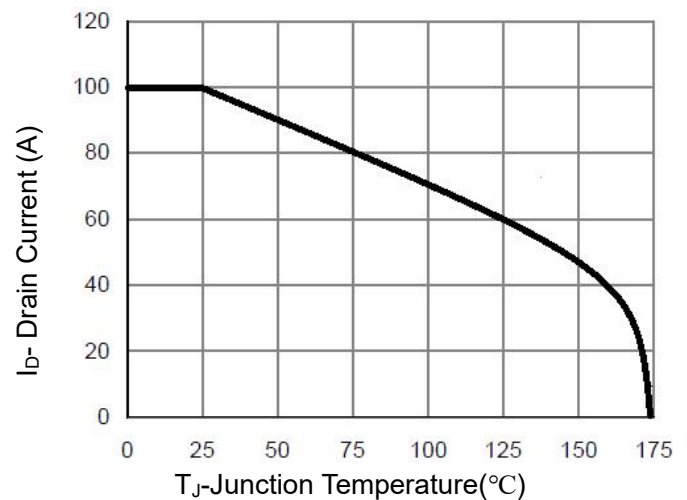


Figure 10 I_D Current De-rating

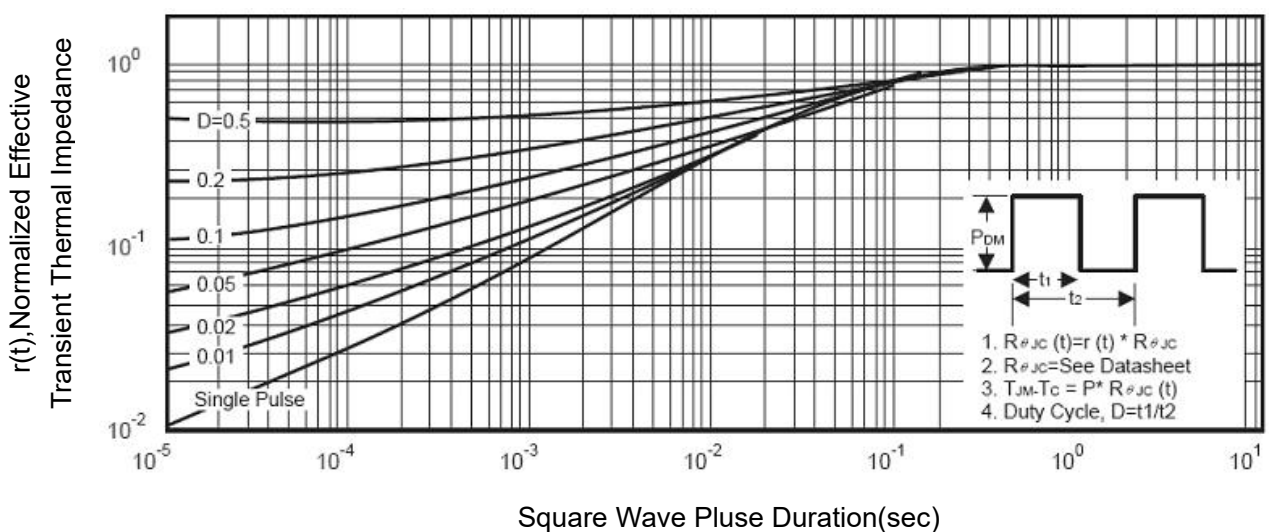
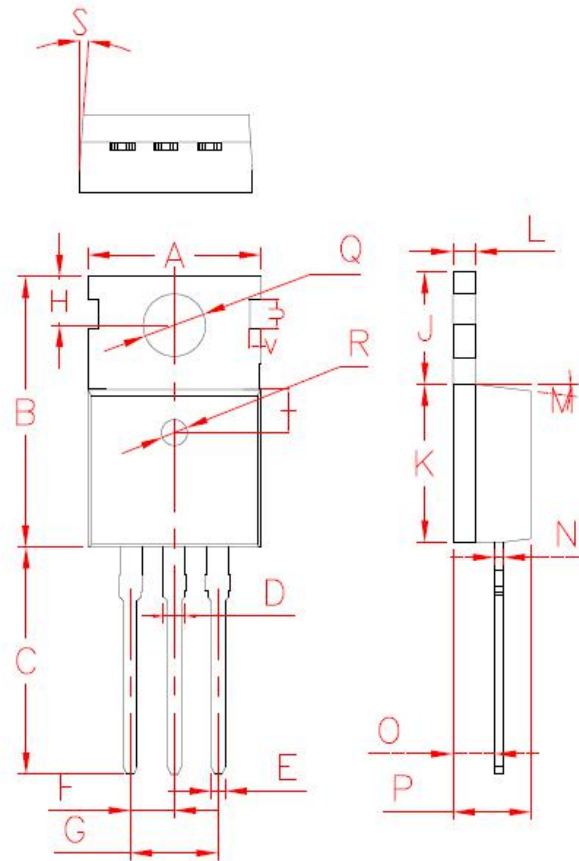


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Min	Non	Max
A	9.80	10.00	10.20
B	15.40	15.60	15.80
C	12.75	13.10	13.45
D	1.18	1.31	1.44
E	0.70	0.80	0.90
F	2.42	2.54	2.66
G	4.84	5.08	5.32
H	2.73	2.80	2.87
I	2.40	2.50	2.60
J	6.40	6.50	6.60
K	9.00	9.10	9.20
L	1.29	1.30	1.32
M	6.5°	7.0°	7.5°
N	0.48	0.50	0.56
O	2.35	2.4	2.5
P	4.4	4.5	4.7
Q	3.5	3.6	3.63
R	1.4	1.5	1.6
S	2°	2.5°	3°
U	1.65	1.75	1.85
V	0.58	0.68	0.78

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