

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE60H15T uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

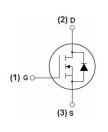
General Features

- V_{DS} =60V, I_{D} =150A $R_{DS(ON)}$ <3.1m Ω @ V_{GS} =10V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

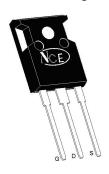
Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED! 100% ΔVds TESTED!



Schematic diagram



TO-247 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE60H15T	NCE60H15T	TO-247	-	-	-

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	60	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	150	Α
Drain Current-Continuous(Tc=100°C)	I _D (100°C)	105	Α
Pulsed Drain Current	I _{DM}	600	Α
Maximum Power Dissipation ^(Note 1)	P _D	220	W
Derating factor		1.47	W/℃
Single pulse avalanche energy (Note 5)	E _{AS}	1950	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 175	$^{\circ}$

Thermal Characteristic



http://www.ncepower.com

NCE60H15T

Thermal Resistance,Junction-to-Case ^(Note 2) R _{θJC} 0.68 °C/W		Rejc	0.68	°C/W
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Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, $I_{D}=250\mu A$	1.3	1.7	2.1	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =75A	-	2.8	3.1	mΩ
Forward Transconductance	g Fs	V _{DS} =10V,I _D =75A	-	75	-	S
Dynamic Characteristics (Note4)	,		'			
Input Capacitance	Clss	V _{DS} =30V,V _{GS} =0V,	-	8730	-	PF
Output Capacitance	Coss		-	625	-	PF
Reverse Transfer Capacitance	Crss	F=1.0MHz	-	599	-	PF
Switching Characteristics (Note 4)		,	'			
Turn-on Delay Time	t _{d(on)}		-	23	-	nS
Turn-on Rise Time	t _r	V_{DD} =30V, R_L =0.4 Ω	-	40	-	nS
Turn-Off Delay Time	t _{d(off)}	V_{GS} =10V, R_{G} =2.5 Ω	-	120	-	nS
Turn-Off Fall Time	t _f		-	33	-	nS
Total Gate Charge	Qg	V _{DS} =30V,I _D =75A,	-	184		nC
Gate-Source Charge	Q _{gs}		-	28		nC
Gate-Drain Charge	Q_{gd}	- V _{GS} =10V	-	40		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =75A	-		1.2	V
Diode Forward Current (Note 2)	Is		-	-	150	Α
Reverse Recovery Time	t _{rr}	TJ = 25°C, IF = 75A	-	54		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	110		nC
Forward Turn-On Time	ton	Intrinsic turn-on time is negl	igible (tur	n-on is do	ominated b	y LS+LD)

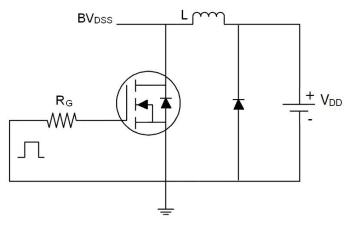
Notes:

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.
- 4. Guaranteed by design, not subject to production
- **5.** EAS condition: Tj=25 $^{\circ}\text{C}$,VDD=30V,VG=10V,L=0.5mH,Rg=25 Ω

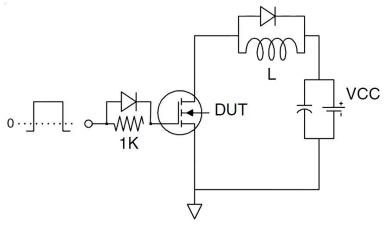


Test circuit

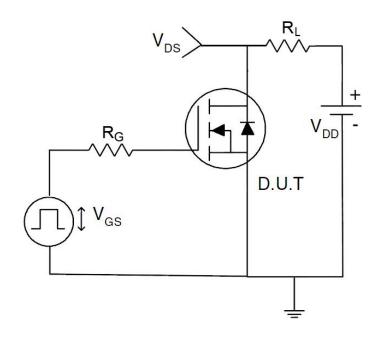
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:





Typical Electrical and Thermal Characteristics (Curves)

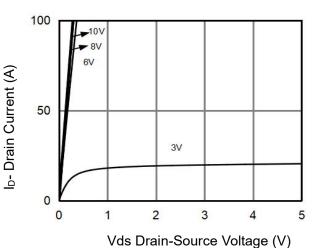
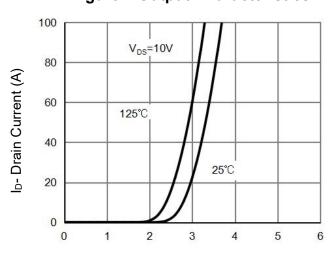


Figure 1 Output Characteristics



Vgs Gate-Source Voltage (V)
Figure 2 Transfer Characteristics

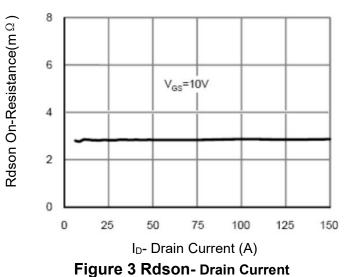


Figure 4 Rdson-JunctionTemperature

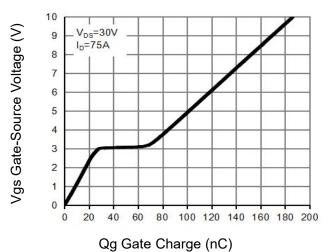


Figure 5 Gate Charge

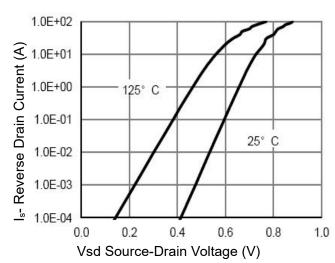


Figure 6 Source- Drain Diode Forward





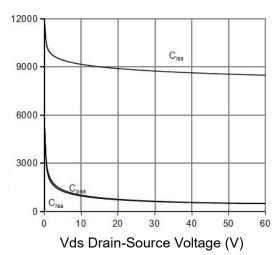


Figure 7 Capacitance vs Vds

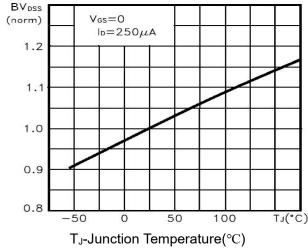


Figure 9 BV_{DSS} vs Junction Temperature

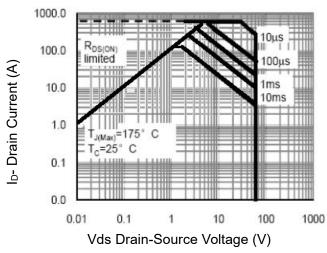
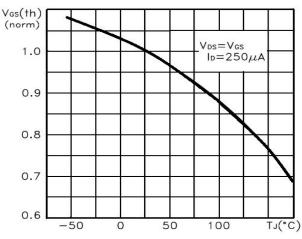


Figure 8 Safe Operation Area



T_J-Junction Temperature(°C)

Figure 10 V_{GS(th)} vs Junction Temperature

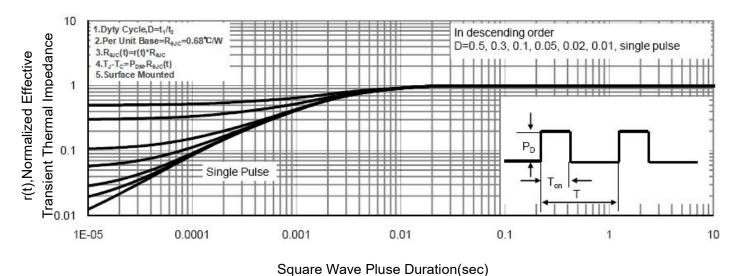
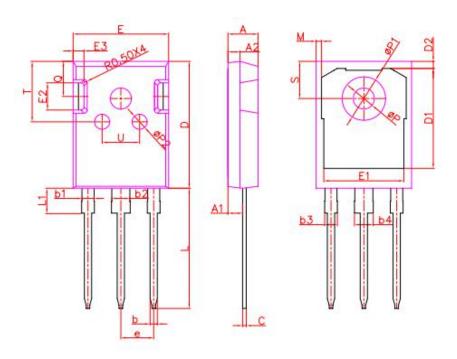


Figure 11 Normalized Maximum Transient Thermal Impedance



TO-247 Package Information



	10	247	
DIM.	MIN.	NOM.	MAX.
Α	4.90	5.00	5.10
A1	2.31	2.432	2.51
A2	1.90	2.00	2.10
b	1.16	1.20	1.26
b1	1.96	2.00	2.06
b2	2.96	3.00	3.06
b3	-	-	2.25
b4	1778	=	3.25
С	0.59	0.60	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.17	1.35
E	15.70	15.80	15.90
E1	13.10	13.26	13.50
E2	4.40	4.50	4.60
E3	1.70	1.80	1.90
е		5.436BSC	
L	19.80	19.90	20.10
L1	_	_	4.30
М	0.35	0.89	0.95
Р	3.40	3.50	3.60
P1	7.00	7.20	7.40
P2	2.40	2.50	2.60
Q	5.60	5.80	6.00
S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40



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