

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE60H18 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

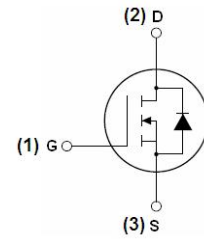
- $V_{DS} = 60V, I_D = 180A$
 $R_{DS(ON)} < 3m\Omega @ V_{GS} = 10V$ (Typ: 2.5m Ω)
- High density cell design for ultra low $R_{DS(ON)}$
- Fully characterized avalanche voltage and current
- Special designed for convertors and power controls
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

- Power switching application
- Hard switched and High frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

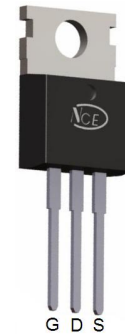
100% ΔV_{DS} TESTED!



Schematic diagram



Marking and pin assignment



TO-220-3L top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE60H18	NCE60H18	TO-220-3L	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	180	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	126	A
Pulsed Drain Current	I_{DM}	540	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.33	W/ $^\circ C$
Single pulse avalanche energy (Note 5)	E_{AS}	1730	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.75	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

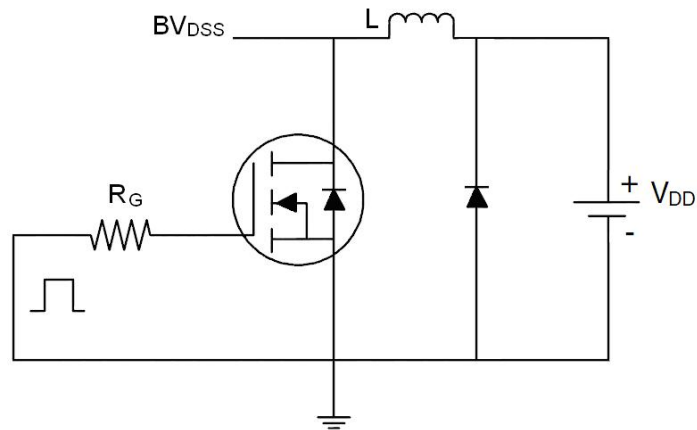
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2	3	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	2.5	3	mΩ
Forward Transconductance	g _{FS}	V _{DS} =20V, I _D =20A	-	60	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	9840	-	PF
Output Capacitance	C _{oss}		-	820	-	PF
Reverse Transfer Capacitance	C _{rss}		-	662	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	VDD=30V, RL=1.5Ω RG=2.5Ω, VGS=10V	-	40	-	nS
Turn-on Rise Time	t _r		-	25	-	nS
Turn-Off Delay Time	t _{d(off)}		-	110	-	nS
Turn-Off Fall Time	t _f		-	30	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =20A, V _{GS} =10V	-	200	-	nC
Gate-Source Charge	Q _{gs}		-	46	-	nC
Gate-Drain Charge	Q _{gd}		-	60	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =20A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	180	A
Reverse Recovery Time	t _{rr}	T _j =25℃, I _F =100A	-		60	nS
Reverse Recovery Charge	Q _{rr}	di/dt=100A/μs (Note3)	-		110	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

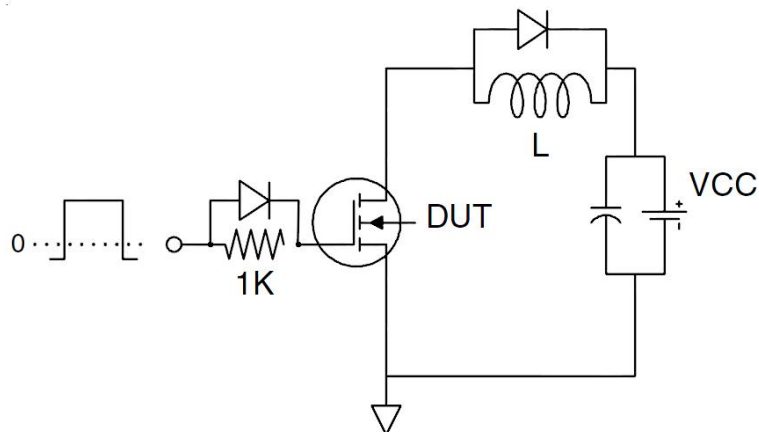
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

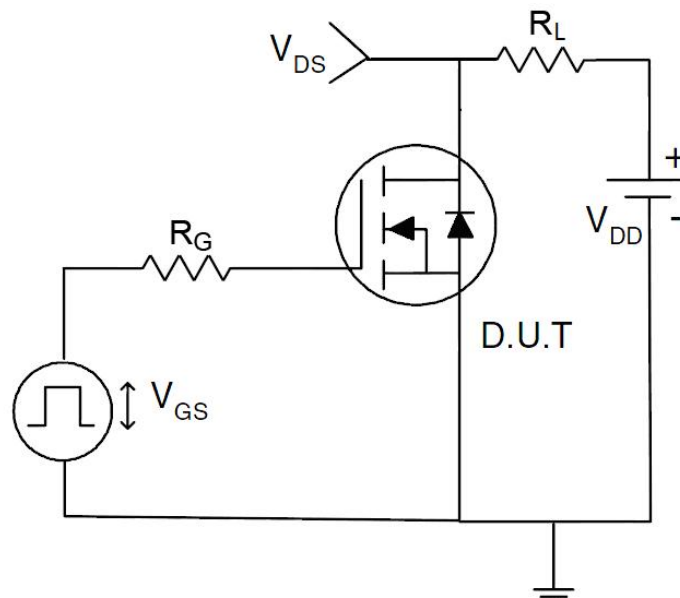
1) EAS Test Circuits



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics (Curves)

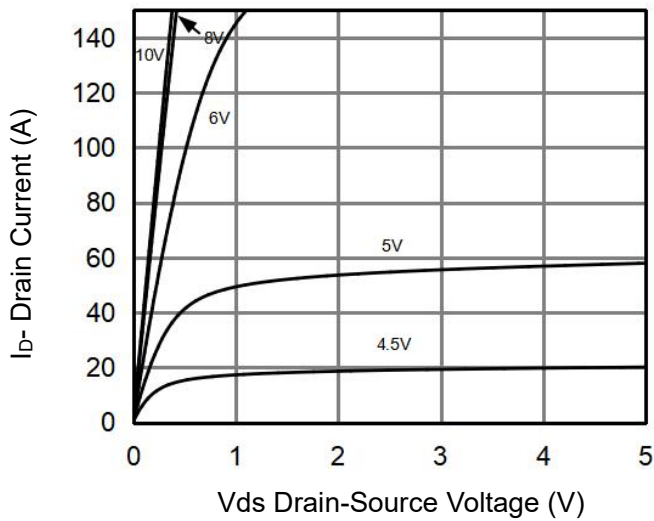


Figure 1 Output Characteristics

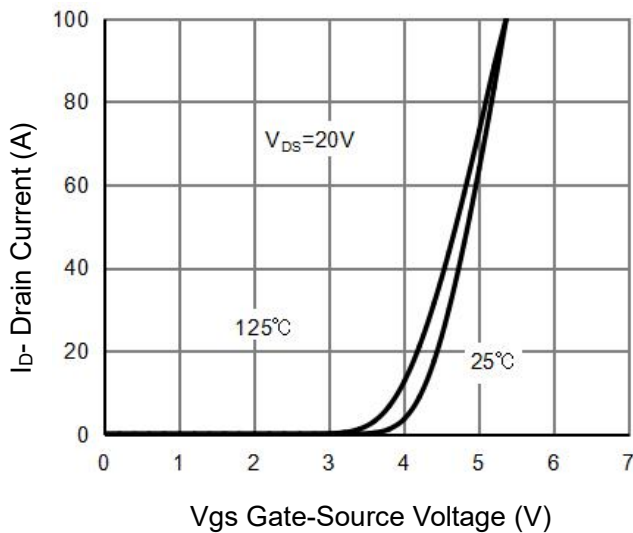


Figure 2 Transfer Characteristics

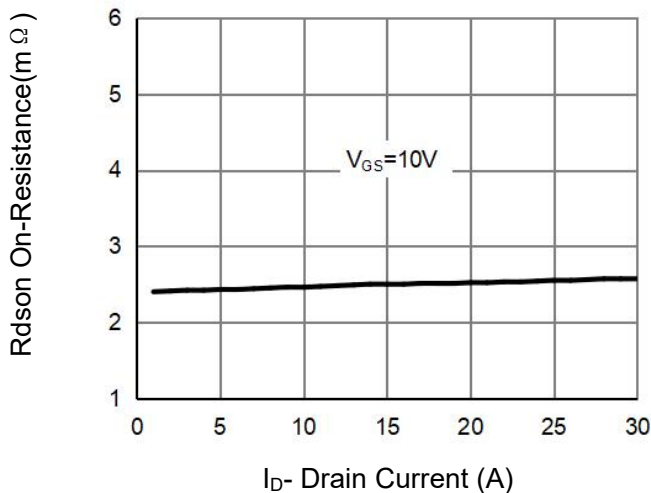


Figure 3 $R_{DS(on)}$ - Drain Current

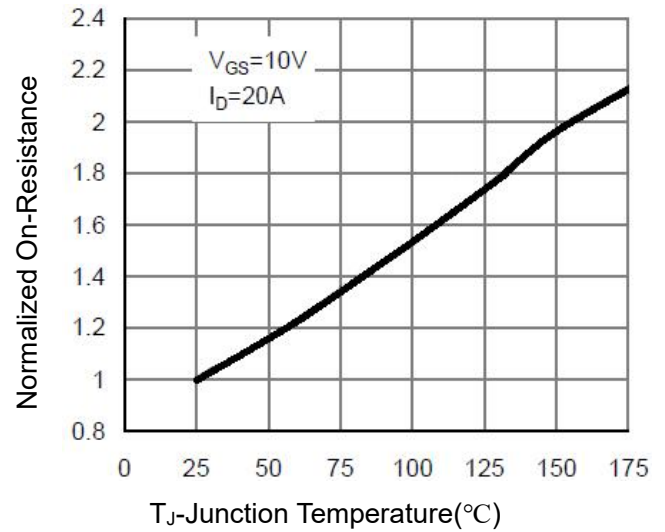


Figure 4 $R_{DS(on)}$ -Junction Temperature

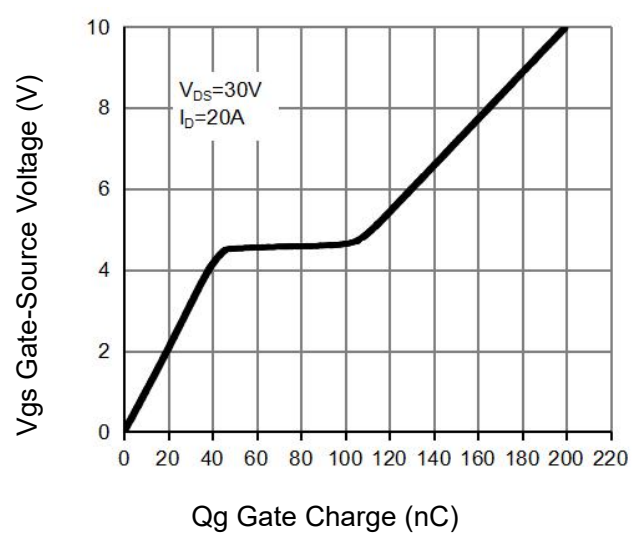


Figure 5 Gate Charge

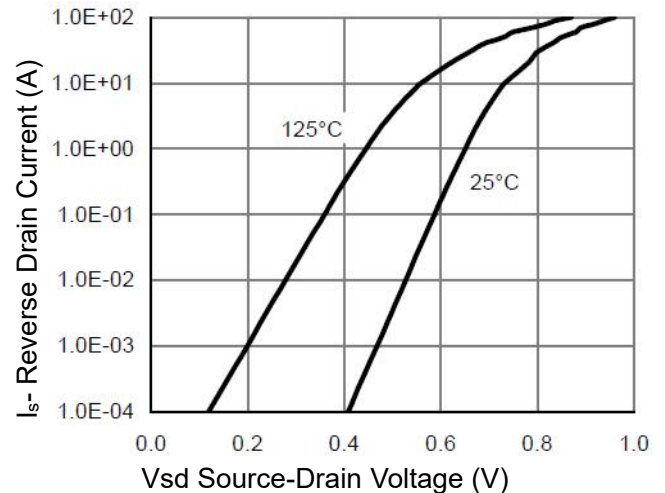


Figure 6 Source- Drain Diode Forward

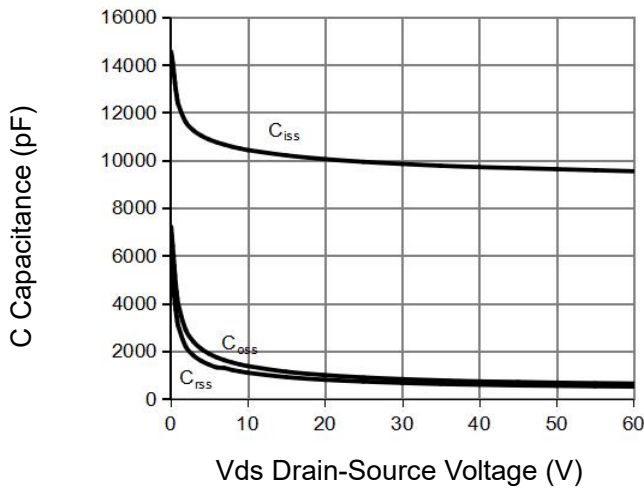


Figure 7 Capacitance vs Vds

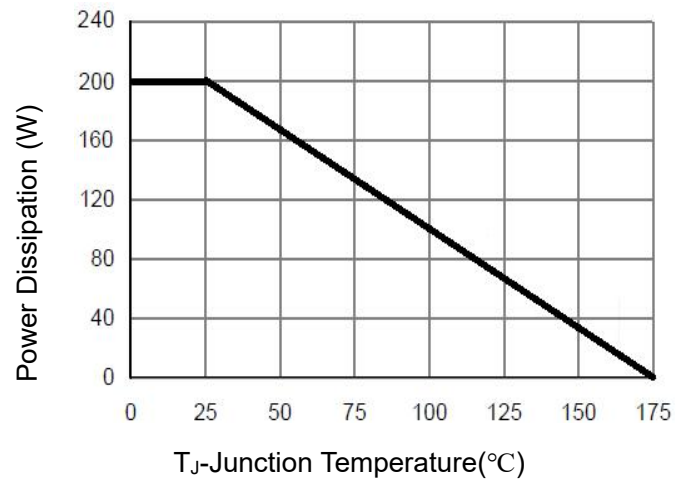


Figure 9 Power De-rating

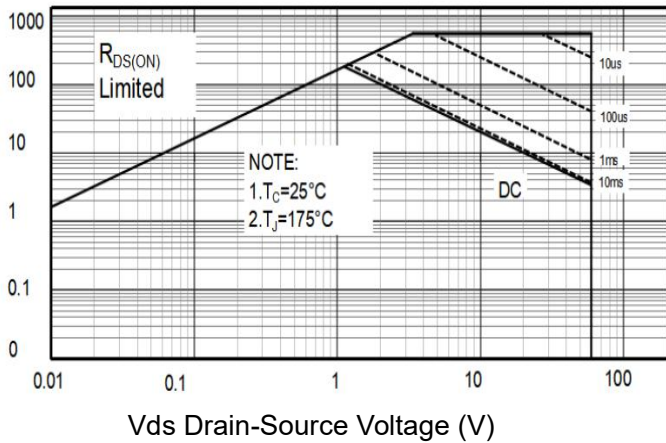


Figure 8 Safe Operation Area

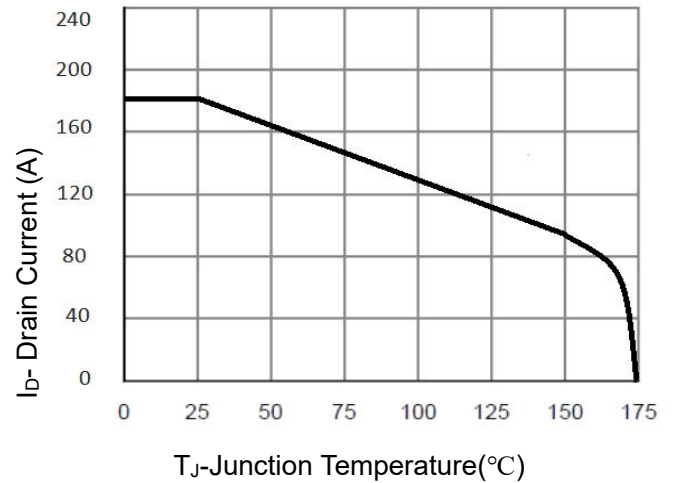


Figure 10 Id Current De-rating

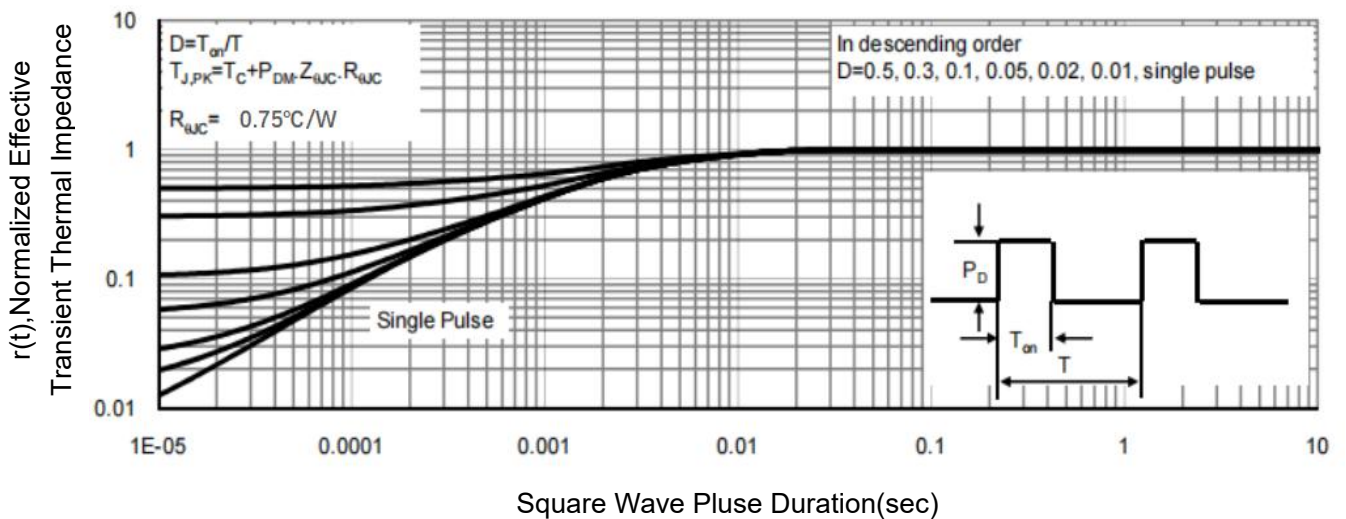
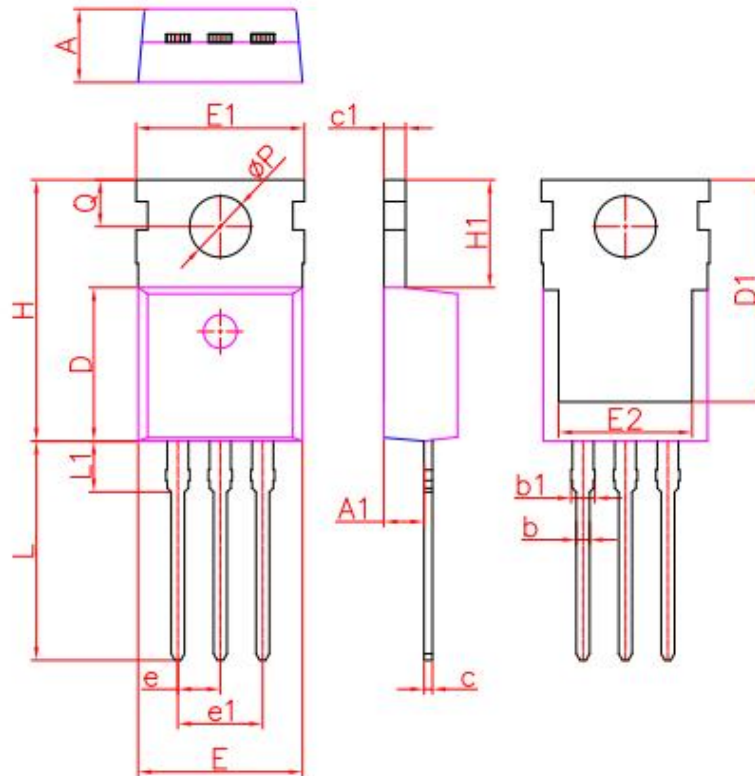


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



TO220			
DIM.	MIN.	NOM.	MAX.
A	4.20	4.40	4.60
A1	2.25	2.40	2.55
b	0.70	0.80	0.90
b1	1.17	1.27	1.37
c	0.33	0.50	0.65
c1	1.20	1.30	1.40
D	8.95	9.20	9.75
D1	13.10	13.30	13.50
E	9.74	9.84	10.04
E1	9.91	10.08	10.25
E2	7.90	8.00	8.10
e	2.54BSC		
e1	5.08BSC		
H	15.45	15.65	15.85
H1	6.30	6.45	6.60
L	12.90	13.13	13.40
L1	2.85	3.05	3.25
Q	2.65	2.80	2.95
øP	3.40	3.68	3.80
All dimensions in millimeters			

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