

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE60H30T uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

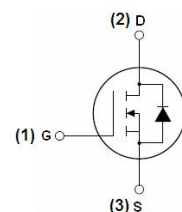
- $V_{DS} = 60V, I_D = 300A$
 $R_{DS(ON)} < 3.1m\Omega @ V_{GS} = 10V$
- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

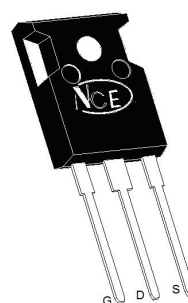
- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic diagram



TO-247 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE60H30T	NCE60H30T	TO-247	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	300	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D (100^\circ C)$	210	A
Pulsed Drain Current	I_{DM}	900	A
Maximum Power Dissipation ^(Note 1)	P_D	400	W
Derating factor		2.67	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	3125	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.38	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

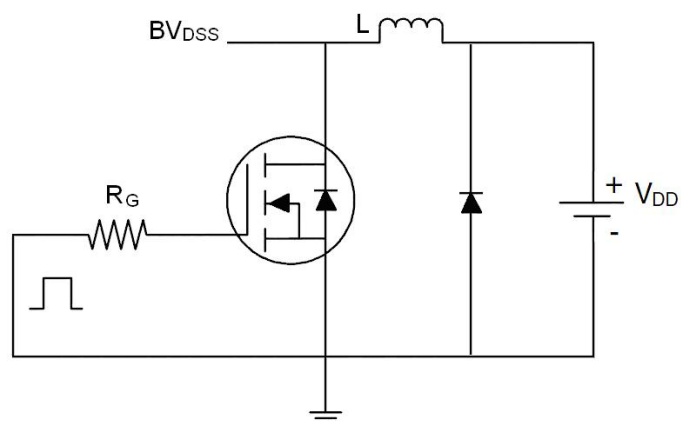
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=60V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.3	1.7	2.1	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=40A$	-	1.8	2.1	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=20V, I_D=40A$	-	120	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C_{iss}	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0MHz$	-	17993	-	PF
Output Capacitance	C_{oss}		-	1255	-	PF
Reverse Transfer Capacitance	C_{rss}		-	992	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, R_L=0.6\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	50	-	nS
Turn-on Rise Time	t_r		-	90	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	280	-	nS
Turn-Off Fall Time	t_f		-	75	-	nS
Total Gate Charge	Q_g	$V_{DS}=30V, I_D=40A,$ $V_{GS}=10V$	-	360		nC
Gate-Source Charge	Q_{gs}		-	61		nC
Gate-Drain Charge	Q_{gd}		-	70		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V_{SD}	$V_{GS}=0V, I_S=40A$	-		1.2	V
Diode Forward Current <small>(Note 2)</small>	I_S		-	-	300	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 40A$ $di/dt = 100A/\mu s$ <small>(Note3)</small>	-	70		nS
Reverse Recovery Charge	Q_{rr}		-	200		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

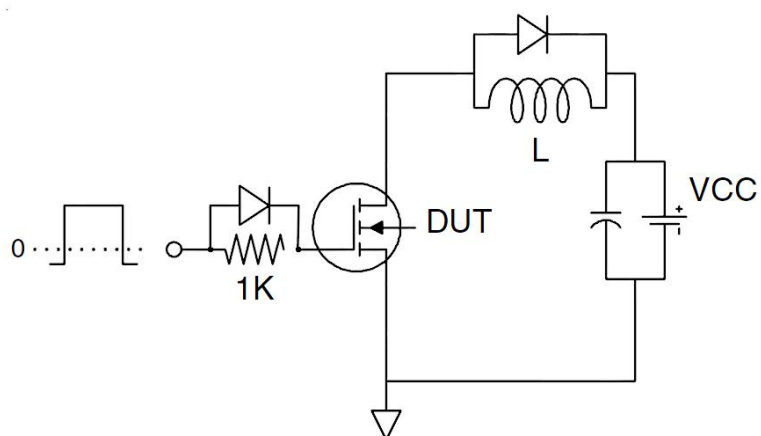
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

Test circuit

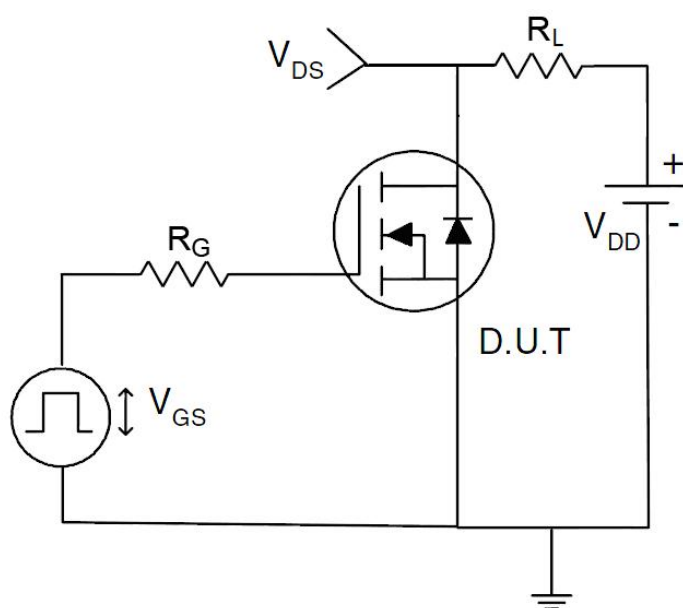
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (Curves)

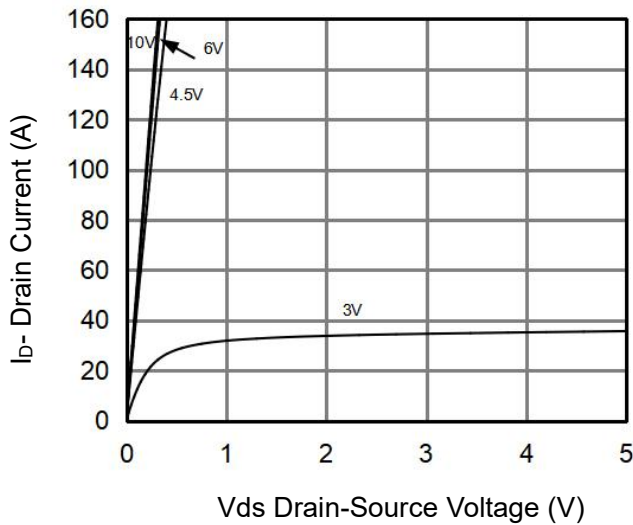


Figure 1 Output Characteristics

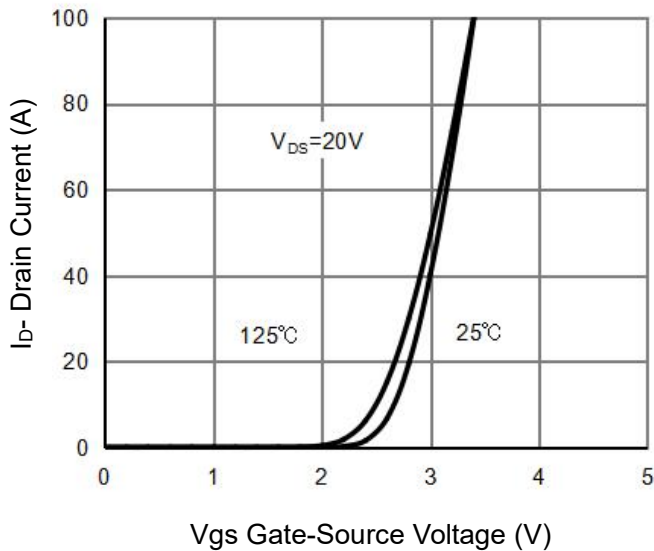


Figure 2 Transfer Characteristics

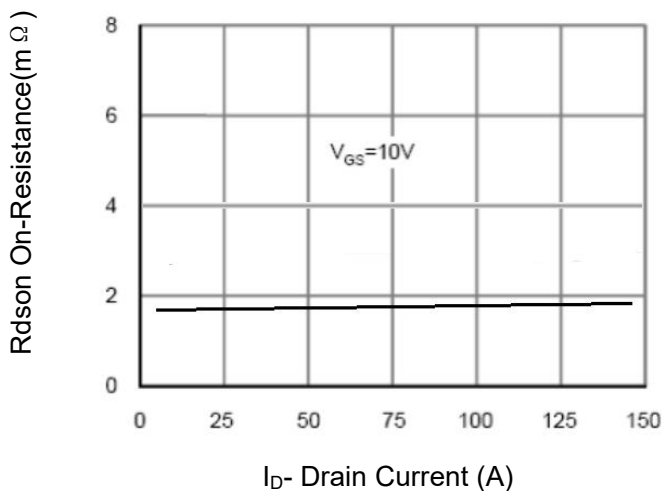


Figure 3 Rdson- Drain Current

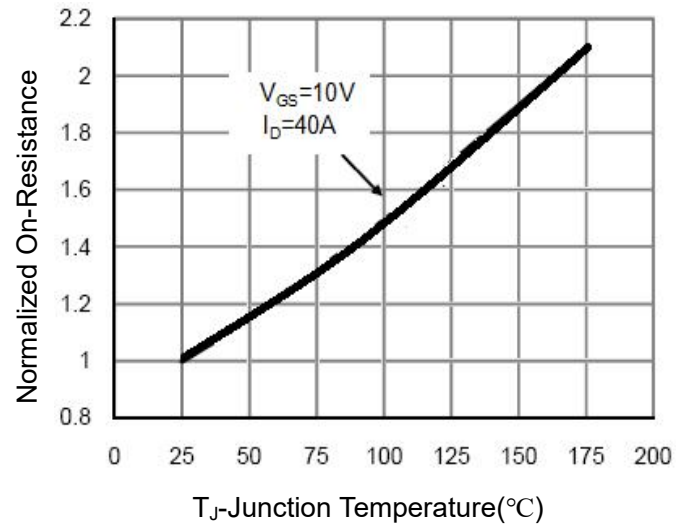


Figure 4 Rdson-Junction Temperature

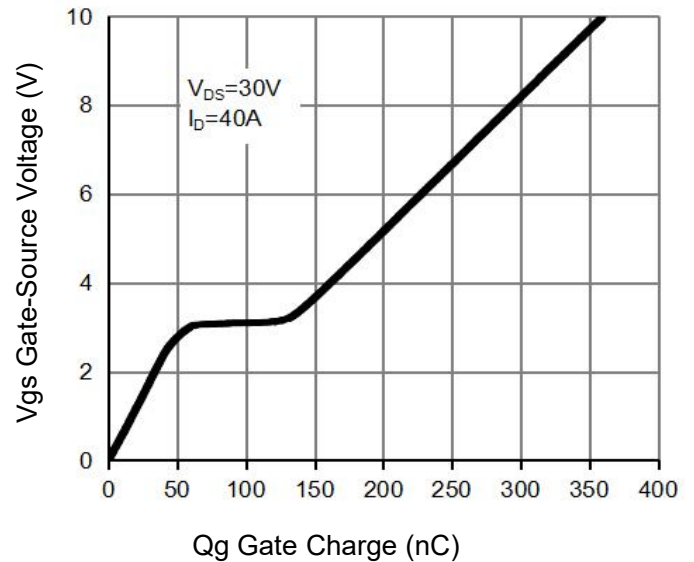


Figure 5 Gate Charge

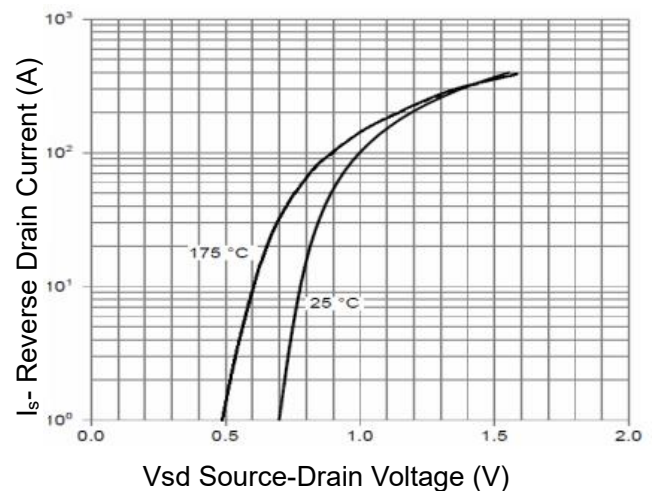


Figure 6 Source- Drain Diode Forward

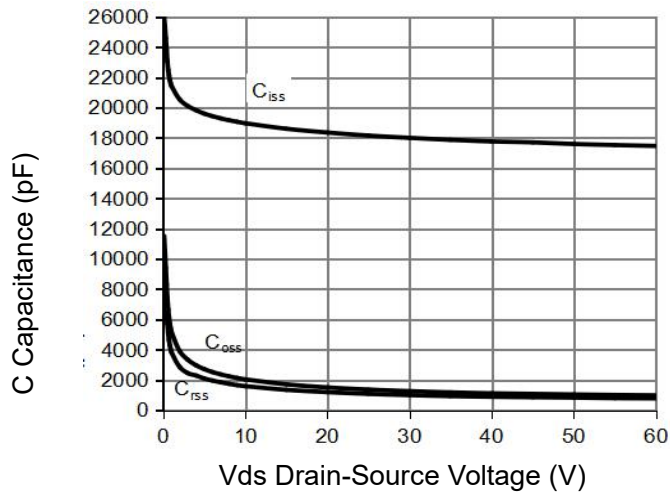


Figure 7 Capacitance vs Vds

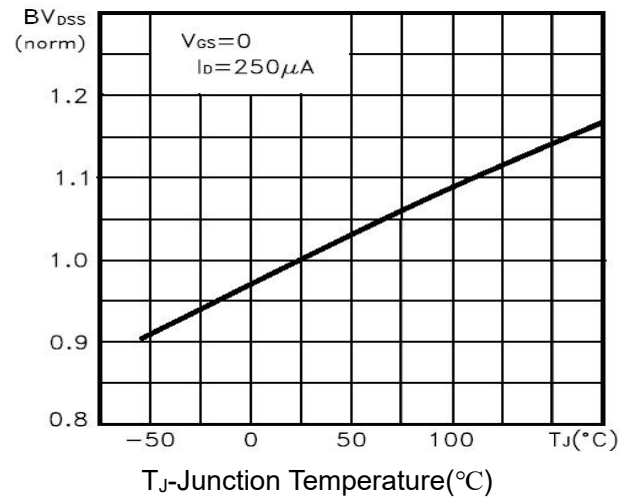


Figure 9 BV_{DSS} vs Junction Temperature

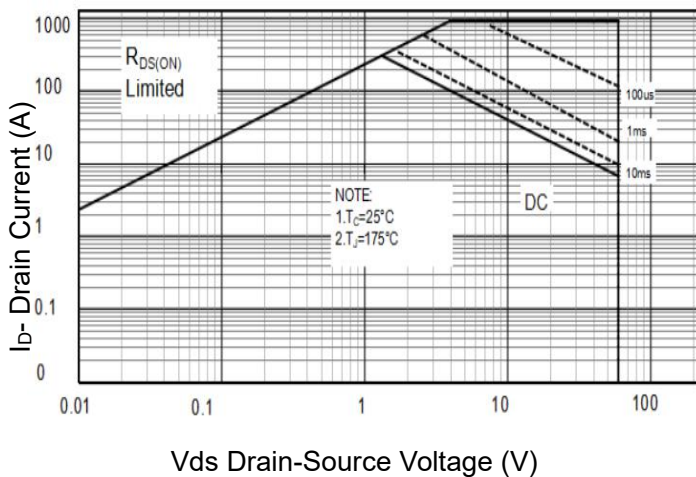


Figure 8 Safe Operation Area

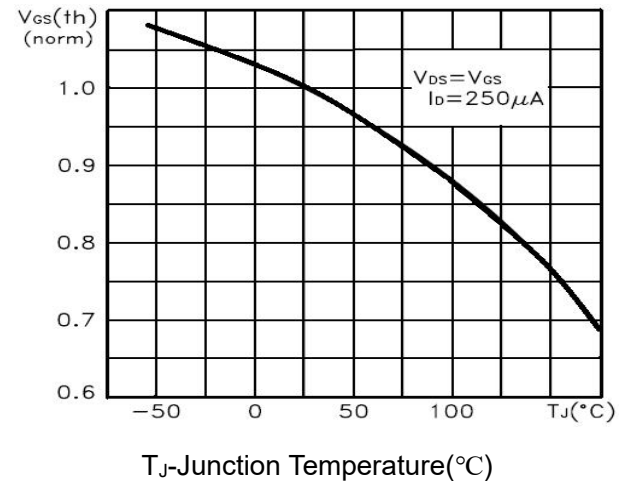


Figure 10 $V_{GS(th)}$ vs Junction Temperature

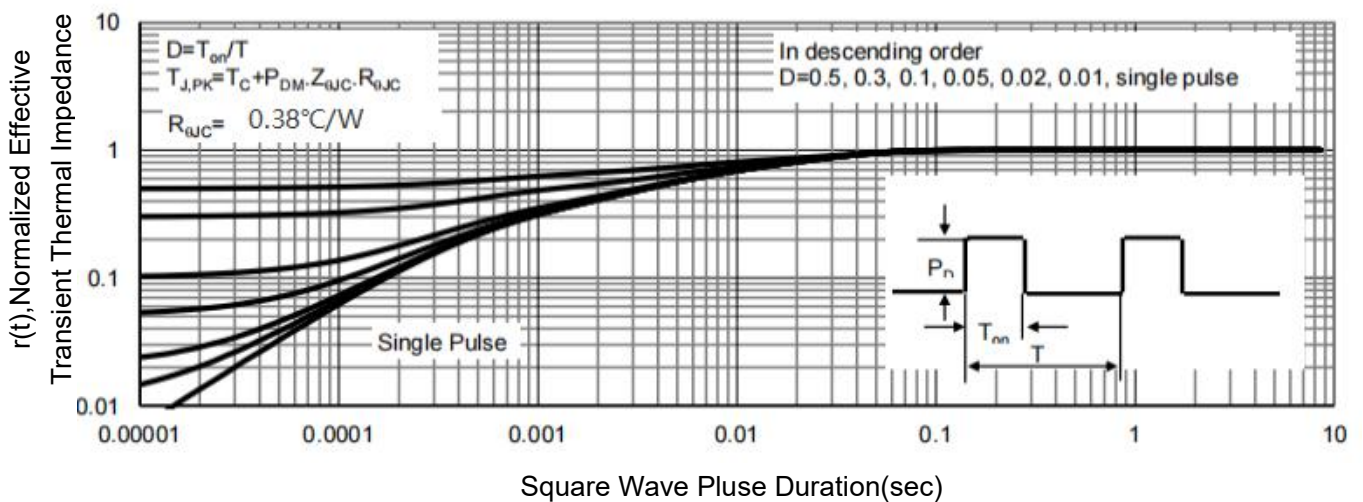
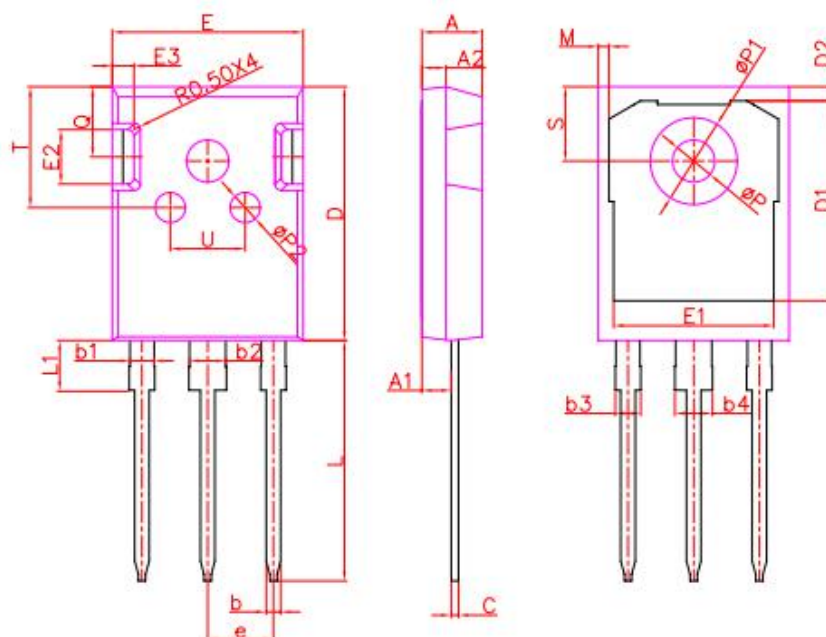


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-247 Package Information



TO247			
DIM.	MIN.	NOM.	MAX.
A	4.90	5.00	5.10
A1	2.31	2.432	2.51
A2	1.90	2.00	2.10
b	1.16	1.20	1.26
b1	1.96	2.00	2.06
b2	2.96	3.00	3.06
b3	—	—	2.25
b4	—	—	3.25
c	0.59	0.60	0.66
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.17	1.35
E	15.70	15.80	15.90
E1	13.10	13.26	13.50
E2	4.40	4.50	4.60
E3	1.70	1.80	1.90
e	5.436BSC		
L	19.80	19.90	20.10
L1	—	—	4.30
M	0.35	0.89	0.95
P	3.40	3.50	3.60
P1	7.00	7.20	7.40
P2	2.40	2.50	2.60
Q	5.60	5.80	6.00
S	6.05	6.15	6.25
T	9.80	10.00	10.20
U	6.00	6.20	6.40
All dimensions in millimeters			

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