N-Channel Super Junction Power MOSFET Ⅳ

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

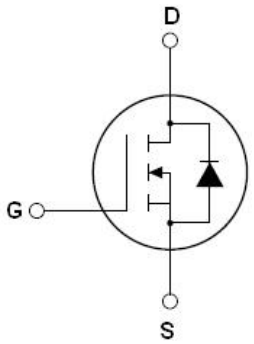
$V_{DS\ min@Tjmax}$	650	V
$R_{DS(ON)TYP}$	145	mΩ
ID	21	A
Qg	23	nC

Features

- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction（PFC）
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply（UPS）
- LLC Half-bridge

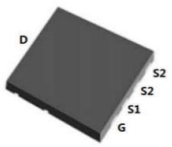


Schematic diagram

✧ **Intrinsic fast-recovery body diode**

Package Marking And Ordering Information

Device	Device Package	Marking
NCE60NF160V	DFN8*8	NCE60NF160V



DFN8×8

Table 1. Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (VGS=0V）	V_{DS}	600	V
Gate-Source Voltage (VDS=0V) AC (f>1 Hz)	V_{GS}	±30	V
Continuous Drain Current at Tc=25°C	$I_{D\ (DC)}$	21	A
Continuous Drain Current at Tc=100°C	$I_{D\ (DC)}$	14.7	A
Pulsed drain current (Note 1)	$I_{DM\ (pluse)}$	63	A
Maximum Power Dissipation(Tc=25°C) Derate above 25°C	P_D	194 1.29	W W/°C
Single pulse avalanche energy (Note 2)	E_{AS}	64	mJ
Avalanche current(Note 1)	I_{AR}	4	A
Repetitive Avalanche energy ， t_{AR} limited by T_{jmax} (Note 1)	E_{AR}	0.35	mJ
Drain Source voltage slope, V_{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt， V_{DS} ≤480 V,I_{SD}<I_D	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55...+175	°C

* limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance，Junction-to-Case（Maximum）	R_{thJC}	0.77	°C /W
Thermal Resistance，Junction-to-Ambient （Maximum）	R_{thJA}	62	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	600			V
Zero Gate Voltage Drain Current(Tc=25℃)	I_{DSS}	V_{DS}=600V,V_{GS}=0V			10	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I_{DSS}	V_{DS}=600V,V_{GS}=0V			200	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	3	4	5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10.5A		145	160	mΩ
Dynamic Characteristics						
Input Capacitance	C_{lss}	V_{DS}=50V,V_{GS}=0V, F=1.0MHz		1200	1400	pF
Output Capacitance	C_{oss}			50		pF
Reverse Transfer Capacitance	C_{rss}			1.5		pF
Total Gate Charge	Q_g	V_{DS}=480V,I_D=10.5A, V_{GS}=10V		23		nC
Gate-Source Charge	Q_{gs}			9		nC
Gate-Drain Charge	Q_{gd}			6.5		nC
Gate plateau voltage	Vgp			6.1		V
Intrinsic gate resistance	R_G	f = 1 MHz open drain		2		Ω
Switching times						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=380V,I_D=10.5A, R_G=1.7Ω,V_{GS}=10V		42		nS
Turn-on Rise Time	t_r			18		nS
Turn-Off Delay Time	$t_{d(off)}$			90		nS
Turn-Off Fall Time	t_f			24		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I_{SD}	T_C=25°C			18	A
Pulsed Source-drain current(Body Diode)	I_{SDM}				54	A
Forward On Voltage	V_{SD}	Tj=25°C,I_{SD}=21A,V_{GS}=0V		0.9	1.2	V
Reverse Recovery Time	t_{rr}	Tj=25°C,I_F=10.5A, di/dt=100A/μs		113		nS
Reverse Recovery Charge	Q_{rr}			0.5		uC
Peak Reverse Recovery Current	I_{rrm}			8		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2. Tj=25℃,VDD=50V,VG=10V, R_G=25Ω

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

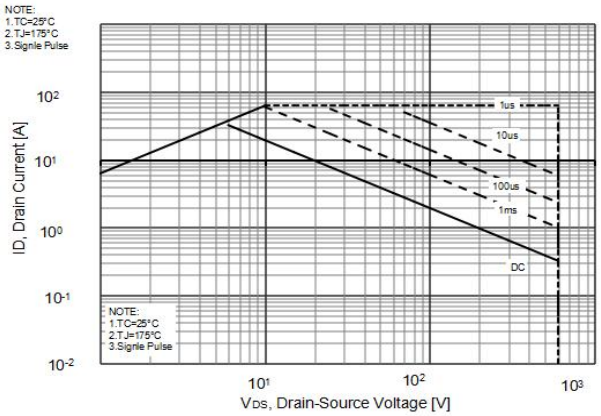


Figure2. Capacitance

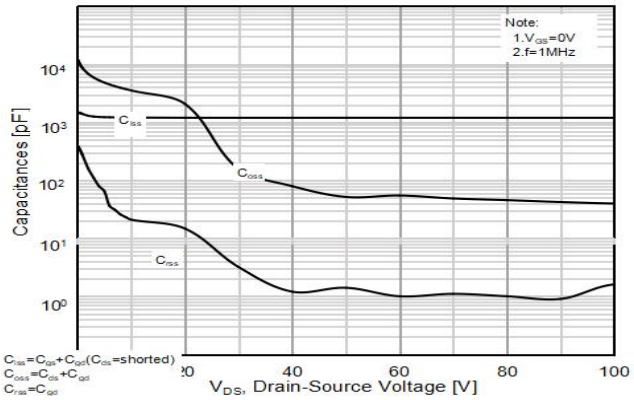


Figure3. Source-Drain Diode Forward Voltage

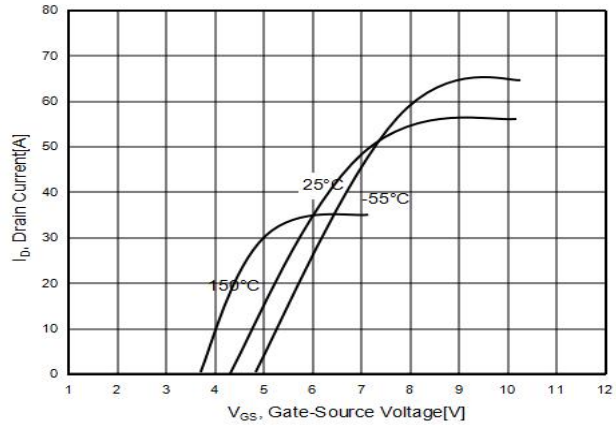


Figure4. Output characteristics

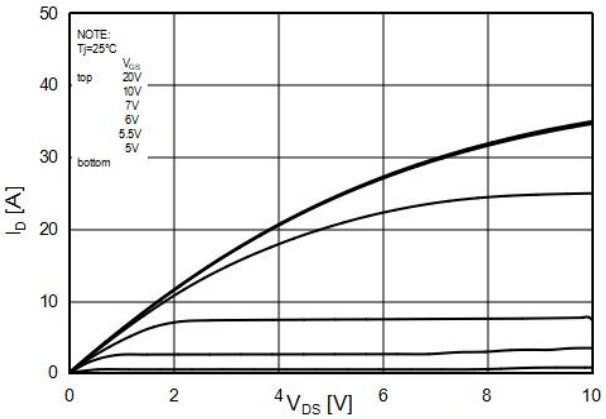


Figure5. $R_{DS(ON)}$ vs Junction Temperature

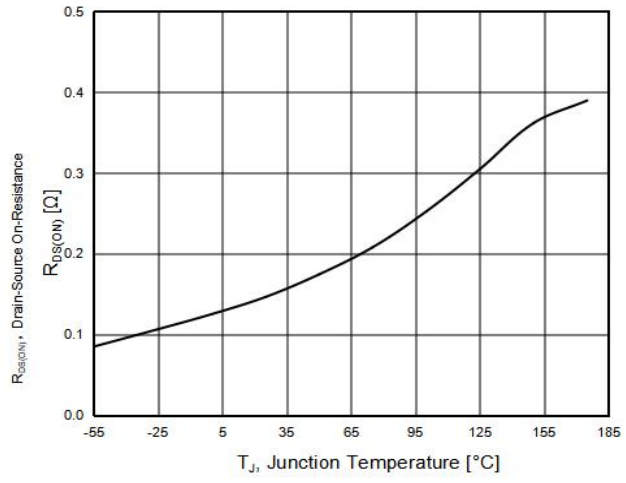


Figure6. BV_{DSS} vs Junction Temperature

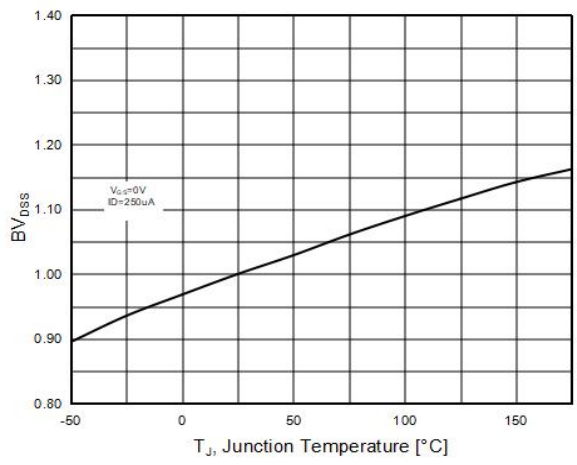


Figure7. Maximum I_D vs Junction Temperature

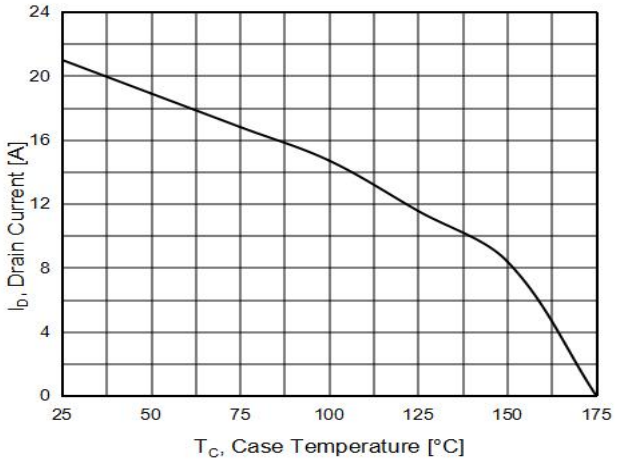


Figure8. Gate charge waveforms

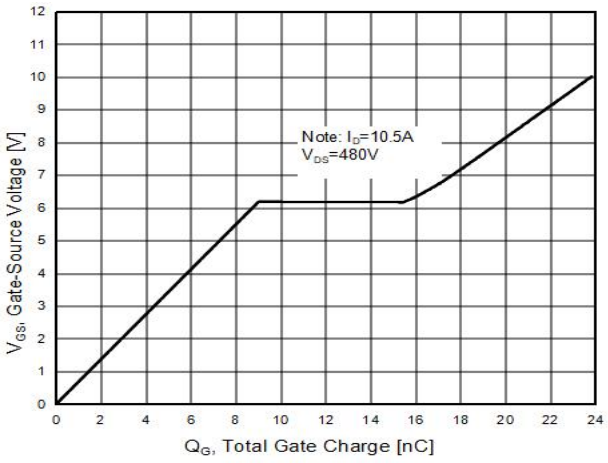


Figure9. Static drain-source on resistance

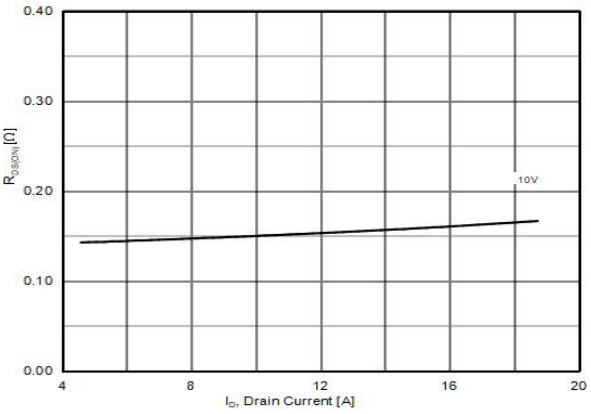
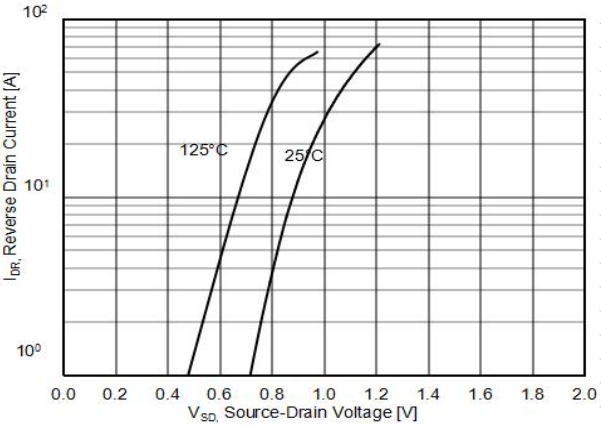
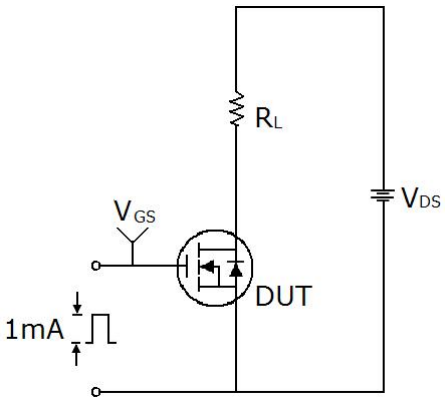


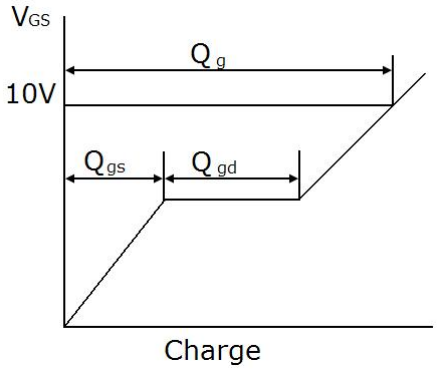
Figure10. Source-Drain Diode Forward Voltage



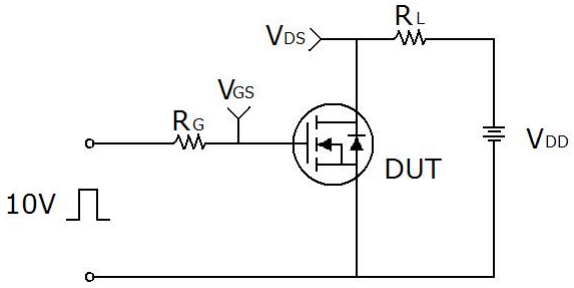
Test circuit

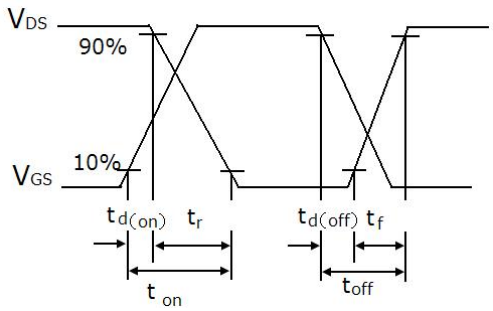
1）Gate charge test circuit & Waveform



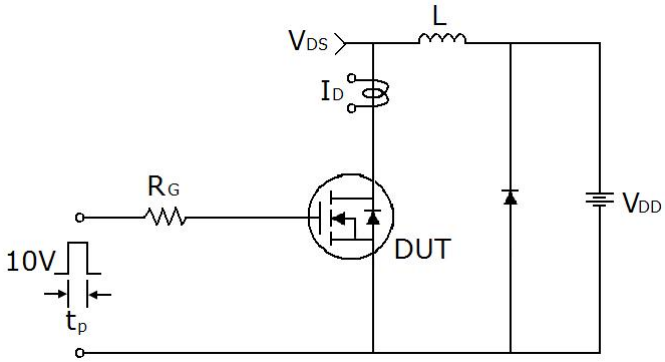


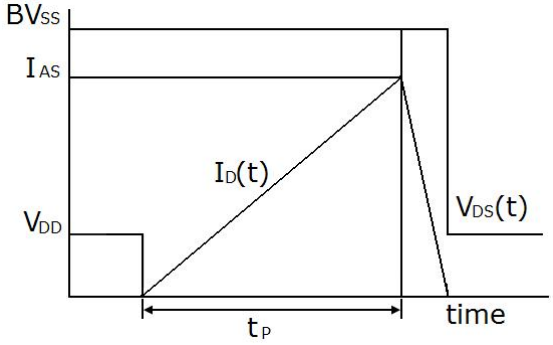
2）Switch Time Test Circuit：



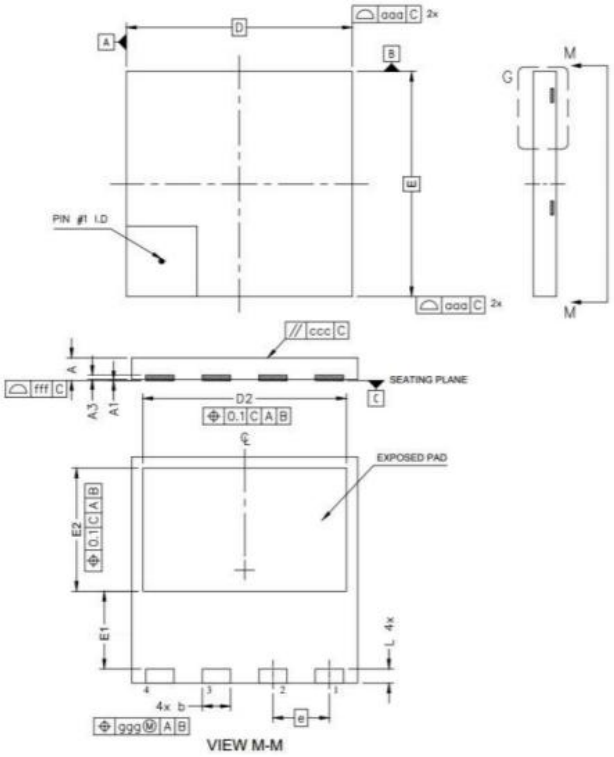


3）Unclamped Inductive Switching Test Circuit & Waveforms





DFN8*8 Package Information



DIM	MIN	NOM	MAX
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e		2.00 BSC	
L	0.40	0.50	0.60
aaa		0.10	
ggg		0.05	
ccc		0.05	
fff		0.05	

NOTES

1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994.

2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

3.0 DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.90mm AND 1.10mm FROM TERMINAL TIP.

4.0 DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH.

5.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.

6.0 RADIUS ON TERMINAL IS OPTIONAL.

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