

N-Channel Super Junction Power MOSFET $\, \mathrm{I\!V}$

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent R_{DS(ON)} with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

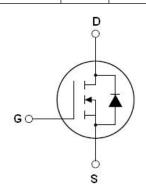
Features

- Optimized body diode reverse recovery performance
- ●Low on-resistance and low conduction losses
- Small package
- ●Ultra Low Gate Charge cause lower driving requirements
- ●100% Avalanche Tested
- ROHS compliant

Дp	plic	ation
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- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge

V _{DS min@Tjmax}	710	V
R _{DS(ON)TYP}	160	mΩ
ID	20	Α
Qg	23	nC



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE65N180	TO-220-3L	NCE65N180



TO-220

Table 1. Absolute Maximum Ratings (T_c=25℃)

Parameter	Symbol	Value	Unit
Drain-Source Voltage (VGS=0V)	VDS	650	V
Gate-Source Voltage (VDS=0V) AC (f>1 Hz)	Vgs	±30	V
Gate-Source Voltage (VDS=0V) DC	Vgs	±20	V
Continuous Drain Current at Tc=25°C	I _{D (DC)}	20	А
Continuous Drain Current at Tc=100°C	I _{D (DC)}	14	А
Pulsed drain current (Note 1)	I _{DM (pluse)}	60	А
Maximum Power Dissipation(Tc=25°C)	P _D	194	W
Derate above 25°C		1.29	w/°C
Single pulse avalanche energy (Note 2)	Eas	144	mJ
Avalanche current ^(Note 1)	I _{AS}	6	А
Repetitive Avalanche energy ,t _{AR} limited by T _{jmax} (Note 1)	Ear	0.73	mJ
Drain Source voltage slope, V _{DS} ≤480 V,	dv/dt	50	V/ns
Reverse diode dv/dt, V _{DS} ≤480 V,I _{SD} <i<sub>D</i<sub>	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T _J ,T _{STG}	-55+175	°C



^{*} limited by maximum junction temperature

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance,Junction-to-Case(Maximum)	R _{thJC}	0.77	°C /W
Thermal Resistance, Junction-to-Ambient (Maximum)	R _{thJA}	62	°C /W

Table 3. Electrical Characteristics (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
On/off states						•
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			1	μΑ
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			100	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250μA	3	3.5	4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =10A		160	180	mΩ
Dynamic Characteristics						
Input Capacitance	C _{lss}	\/ F0\/\/ 0\/		1200	1400	pF
Output Capacitance	Coss	V_{DS} =50V, V_{GS} =0V, F=1.0MHz		50		pF
Reverse Transfer Capacitance	C _{rss}	F=1.0IVIH2		1.5		pF
Total Gate Charge	Qg			23		nC
Gate-Source Charge	Q _{gs}	V _{DS} =480V,I _D =10.5A,		9		nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V		6.5		nC
Gate plateau voltage	Vgp			6.1		V
Intrinsic gate resistance	R _G	f = 1 MHz open drain		2		Ω
Switching times	·					
Turn-on Delay Time	t _{d(on)}			32		nS
Turn-on Rise Time	t _r	V _{DD} =380V,I _D =10A,		18		nS
Turn-Off Delay Time	t _{d(off)}	$R_G=1.7\Omega, V_{GS}=10V$		90		nS
Turn-Off Fall Time	t _f			8		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T -25°C			20	Α
Pulsed Source-drain current(Body Diode)	I _{SDM}	T _C =25°C			60	Α
Forward On Voltage	V _{SD}	Tj=25°C,I _{SD} =20A,V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	Ti=25°C L =40A		300		nS
Reverse Recovery Charge	Qrr	Tj=25°C,I _F =10A, di/dt=100A/μs		4.5		uC
Peak Reverse Recovery Current	I _{rrm}	ui/ut-100A/µS		30		Α

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

^{2.} Tj=25°C,VDD=50V,VG=10V, R_G=25 Ω



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure 1. Safe operating area

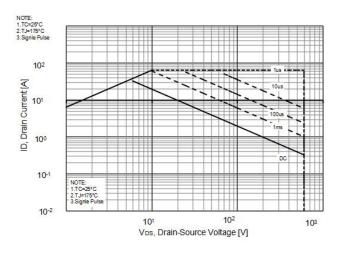


Figure 2. Capacitance

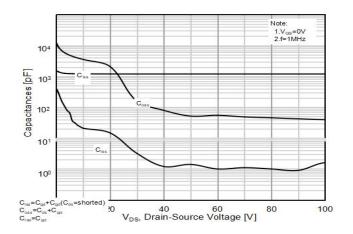


Figure 3. Source-Drain Diode Forward Voltage

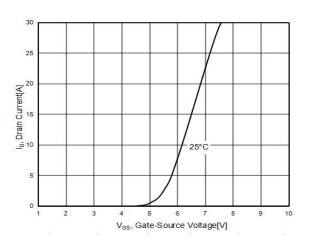


Figure 4. Output characteristics

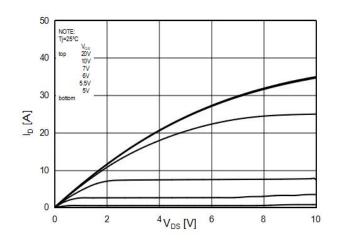


Figure 5. R_{DS(ON)} vs Junction Temperature

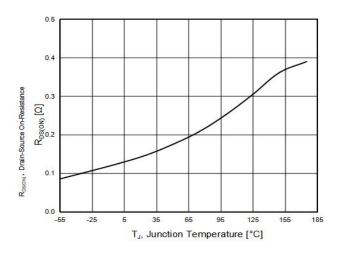


Figure 6. BV_{DSS} vs Junction Temperature

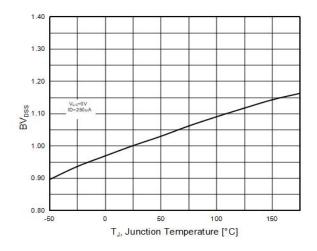




Figure 7. Maximum I_D vs Junction Temperature

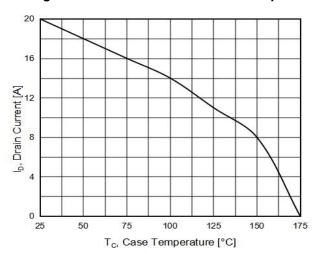


Figure8. Gate charge waveforms

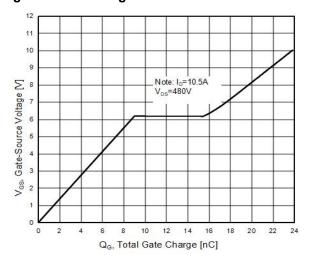


Figure 9. Static drain-source on resistance

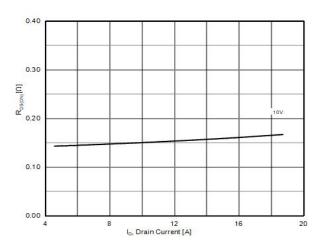
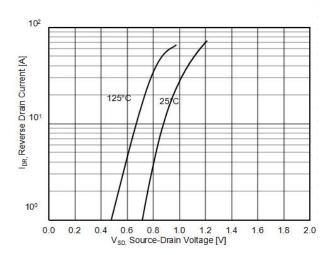


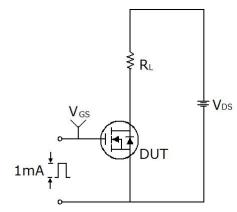
Figure 10. Source-Drain Diode Forward Voltage

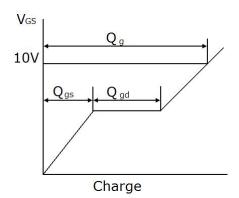




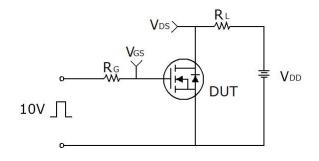
Test circuit

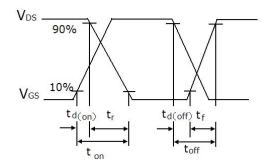
1) Gate charge test circuit & Waveform



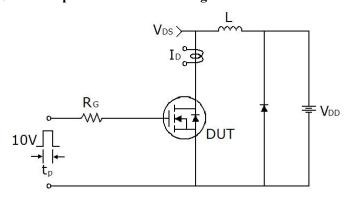


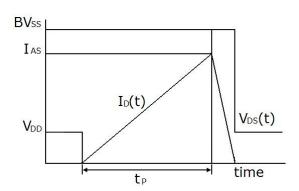
2) Switch Time Test Circuit:





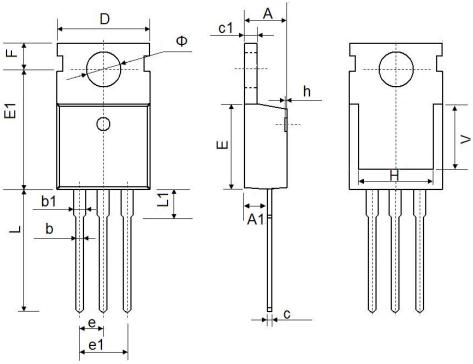
3) Unclamped Inductive Switching Test Circuit & Waveforms







TO-220 Package Information



Comphal	Dimensions	In Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	4.400	4.600	0.173	0.181	
A1	2.250	2.550	0.089	0.100	
b	0.710	0.910	0.028	0.036	
b1	1.170	1.370	0.046	0.054	
С	0.330	0.650	0.013	0.026	
c1	1.200	1.400	0.047	0.055	
D	9.910	10.250	0.390	0.404	
E	8.9500	9.750	0.352	0.384	
E1	12.650	12.950	0.498	0.510	
е	2.540	TYP.	0.100 TYP.		
e1	4.980	5.180	0.196	0.204	
F	2.650	2.950	0.104	0.116	
Н	7.900	8.100	0.311	0.319	
h	0.000	0.300	0.000	0.012	
L	12.900	13.400	0.508	0.528	
L1	2.850	3.250	0.112	0.128	
V	7.500	7.500 REF.		REF.	
Ф	3.400	3.800	0.134	0.150	

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