

N-Channel Super Junction Power MOSFET IV

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

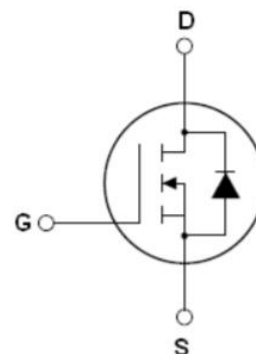
Features

- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge

$V_{DS\ min@T_{jmax}}$	710	V
$R_{DS(ON)TYP.}$	790	mΩ
I_D	5.1	A
Q_g	9	nC



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE65N900D	TO-263-2L	NCE65N900D



TO-263

Table 1. Absolute Maximum Ratings ($T_c=25^{\circ}C$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	650	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1\ Hz$)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$), DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^{\circ}C$	$I_{D(DC)}$	5.1	A
Continuous Drain Current at $T_c=100^{\circ}C$	$I_{D(DC)}$	3.57	A
Pulsed drain current (Note 1)	$I_{DM(pluse)}$	15.3	A
Maximum Power Dissipation($T_c=25^{\circ}C$)	P_D	59	W
Derate above $25^{\circ}C$		0.39	W/ $^{\circ}C$
Single pulse avalanche current (Note 2)	I_{AS}	1.5	A
Reverse diode dv/dt, $V_{DS} \leq 480\ V, I_{SD} < I_D$	dv/dt	50	V/ns
Drain Source voltage slope, $V_{DS} \leq 480\ V$	dv/dt	15	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55...+175	$^{\circ}C$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	2.54	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250uA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =650V,V _{GS} =0V			50	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±200	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250uA	3		4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =2.5A		790	900	mΩ
Dynamic Characteristics						
Gate Resistance	R _g	F=1MHZ, D-S short		36		Ω
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V, F=1MHz		296		pF
Output Capacitance	C _{oss}			12		pF
Reverse Transfer Capacitance	C _{rss}			4		pF
Total Gate Charge	Q _g	V _{DS} =480V,I _D =2.5A, V _{GS} =10V		9		nC
Gate-Source Charge	Q _{gs}			2.3		nC
Gate-Drain Charge	Q _{gd}			3.2		nC
Gate plateau voltage	V _{gp}			5.7		V
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =480V,I _D =2.5A, R _G =4Ω,V _{GS} =10V		7		nS
Turn-on Rise Time	t _r			3		nS
Turn-Off Delay Time	t _{d(off)}			50		nS
Turn-Off Fall Time	t _f			9		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			5.1	A
Pulsed-Source-drain current(Body Diode)	I _{SDM}				15.3	A
Forward on voltage	V _{SD}	T _j =25℃,I _{SD} =5.1A,V _{GS} =0V		0.9	1.1	V
Reverse Recovery Time	t _{rr}	T _j =25℃,I _F 2.5A, di/dt=100A/μs		190		nS
Reverse Recovery Charge	Q _{rr}			0.57		uC
Peak reverse recovery current	I _{rrm}			6		A

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

Figure1. Safe operating area

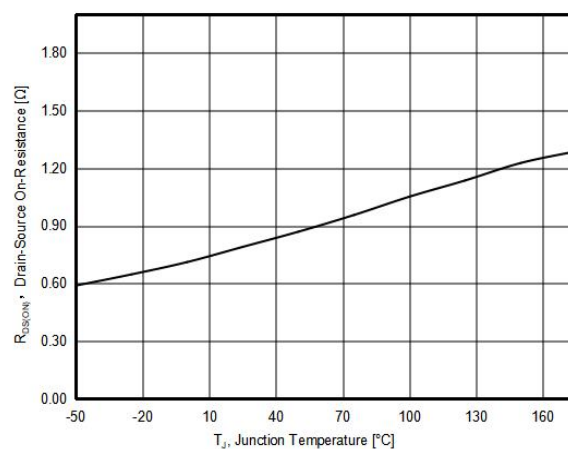


Figure7. BV_{DSS} vs Junction Temperature

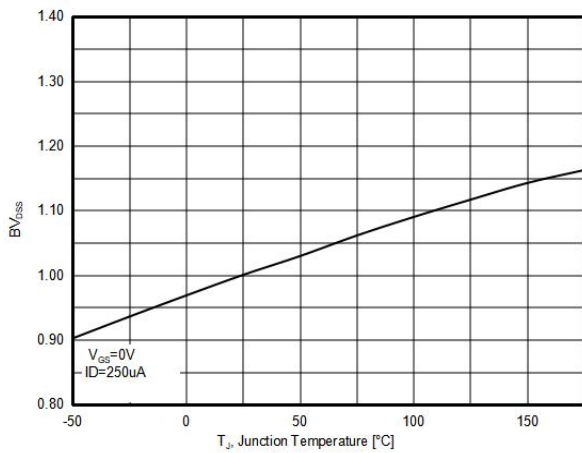


Figure8. Maximum I_D vs Junction Temperature

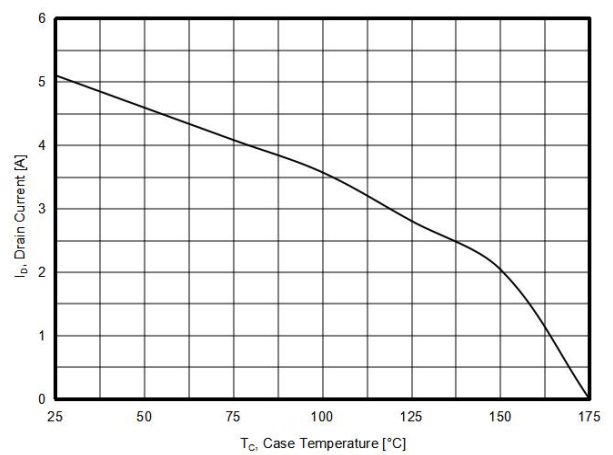


Figure9. Gate charge waveforms

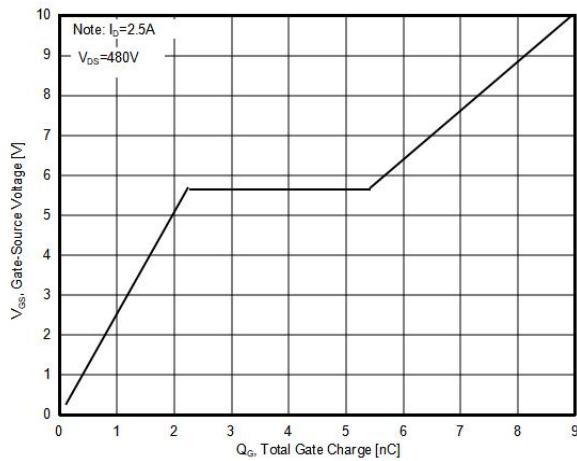
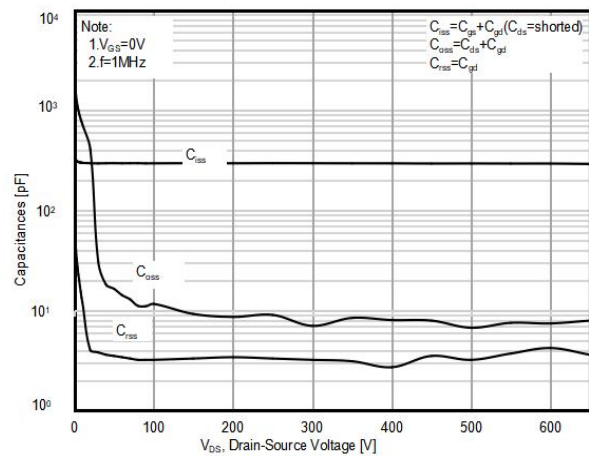
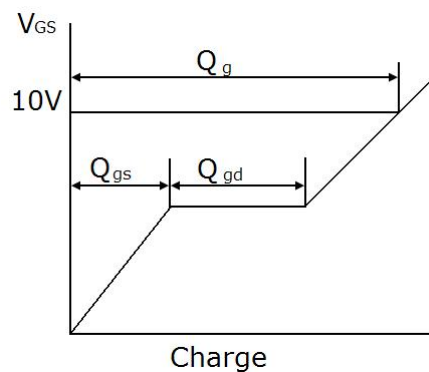
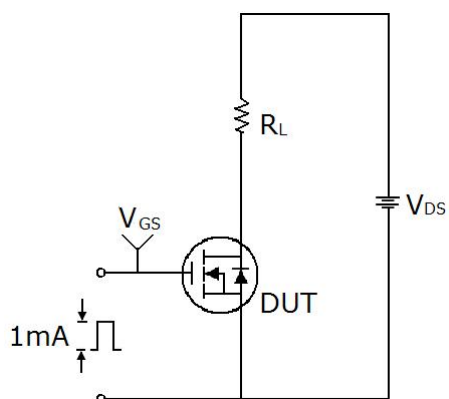


Figure10. Capacitance

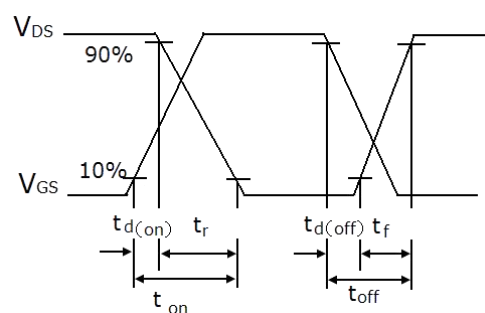
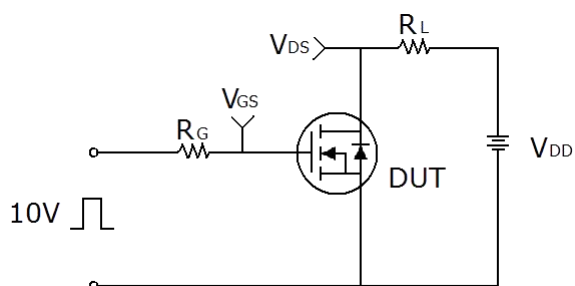


Test circuit

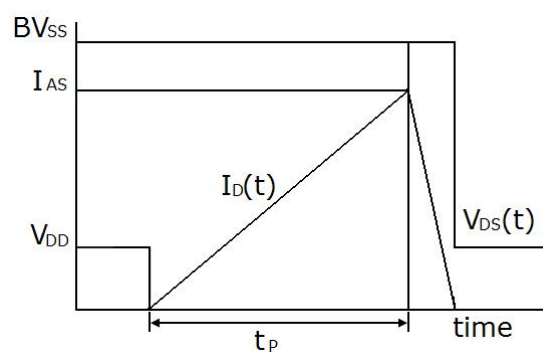
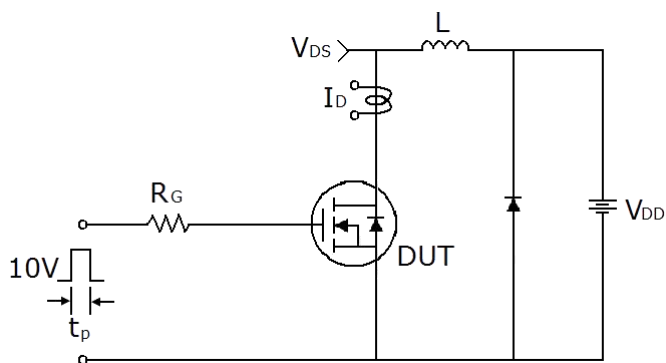
1) Gate charge test circuit & Waveform



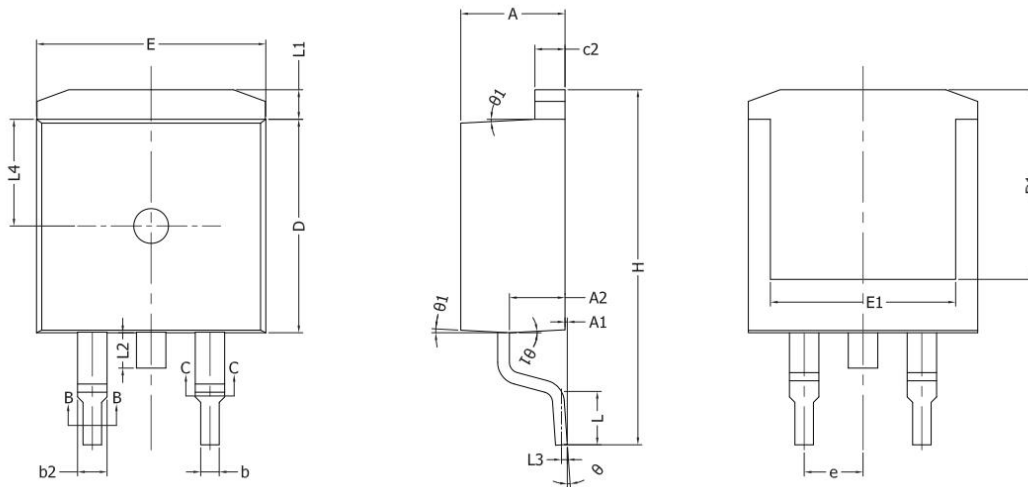
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



TO-263-P Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.40	4.60	0.173	0.181
A1	0.00	0.25	0.000	0.010
A2	2.20	2.60	0.087	0.102
b	0.76	0.89	0.030	0.035
b1	0.75	0.85	0.030	0.033
b2	1.23	1.37	0.048	0.054
b3	1.22	1.32	0.048	0.052
c	0.47	0.60	0.019	0.024
c1	0.46	0.56	0.018	0.022
c2	1.25	1.35	0.049	0.053
D	9.10	9.30	0.358	0.366
D1	8.00		0.315	
E	9.80	10.00	0.386	0.394
E1	7.80		0.307	
e	2.54BSC		0.100BSC	
H	14.90	15.70	0.587	0.618
L	2.00	2.60	0.079	0.102
L1	1.17	1.40	0.046	0.055
L2		1.75		0.069
L3	0.25BSC		0.101BSC	
L4	4.60REF		0.181REF	

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