

## N-Channel Super Junction Power MOSFET IV

### General Description

The series of devices use advanced trench gate super junction technology and design to provide ultra-low  $R_{DS(ON)}$  and low gate charge and With a rapid recovery body diode. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, industrial power applications, Fast charger, new energy vehicle charging pile, on-board OBC etc.

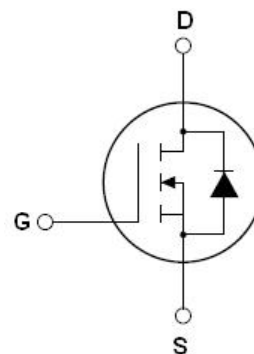
### Features

- New technology for high voltage device
- Ultra low on-resistance and ultra low conduction losses
- Ultra Low Gate Charge cause lower driving requirements
- Diode reverse recovery speed is super fast
- High reliability
- ROHS compliant & Halogen Free

### Application

- Power factor correction (PFC)
- Switched mode power supplies (SMPS)
- Uninterruptible Power Supply (UPS)
- On-board charger (OBC)

$V_{DS \min @ T_{jmax}}$	710	V
$R_{DS(ON)TYP}$	110	mΩ
$I_D$	26	A
$Q_g$	41	nC



Schematic diagram

✧ Intrinsic fast-recovery body diode

### Package Marking And Ordering Information

Device	Device Package	Marking
NCE65NF130V	DFN8*8	NCE65NF130V

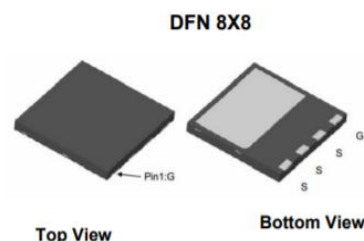


Table 1. Absolute Maximum Ratings ( $T_c=25^\circ\text{C}$ )

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS}=0V$ )	$V_{DS}$	650	V
Gate-Source Voltage ( $V_{DS}=0V$ ) AC ( $f>1\text{ Hz}$ )	$V_{GS}$	$\pm 30$	V
Gate-Source Voltage ( $V_{DS}=0V$ ) DC	$V_{GS}$	$\pm 20$	V
Continuous Drain Current at $T_c=25^\circ\text{C}$	$I_D (DC)$	26	A
Continuous Drain Current at $T_c=100^\circ\text{C}$	$I_D (DC)$	18.2	A
Pulsed drain current (Note 1)	$I_{DM (pluse)}$	78	A
Maximum Power Dissipation ( $T_c=25^\circ\text{C}$ )	$P_D$	237	W
Derate above $25^\circ\text{C}$		1.58	W/ $^\circ\text{C}$
Avalanche current (Note 1)	$I_{AS}$	7	A
Drain Source voltage slope, $V_{DS} \leq 480\text{ V}$ ,	$dv/dt$	50	V/ns
Reverse diode $dv/dt$ , $V_{DS} \leq 480\text{ V}$ , $I_{SD} < I_D$	$dv/dt$	50	V/ns
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55...+175	$^\circ\text{C}$

\* limited by maximum junction temperature

**Table 2. Thermal Characteristic**

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	$R_{thJC}$	0.63	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	$R_{thJA}$	62	$^{\circ}\text{C}/\text{W}$

**Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)**

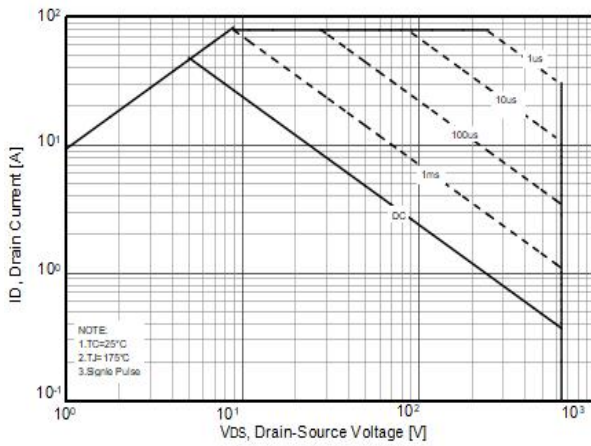
Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250uA	650			V
Zero Gate Voltage Drain Current(Tc=25℃)	I <sub>DSS</sub>	V <sub>DS</sub> =650V,V <sub>GS</sub> =0V			10	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I <sub>DSS</sub>	V <sub>DS</sub> =650V,V <sub>GS</sub> =0V			400	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =500uA	3.5	4.2	5.0	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =13A		110	130	mΩ
Dynamic Characteristics						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V,V <sub>GS</sub> =0V, F=1.0MHz		2161		pF
Output Capacitance	C <sub>oss</sub>			95		pF
Reverse Transfer Capacitance	C <sub>rss</sub>			50		pF
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =480V,I <sub>D</sub> =13A, V <sub>GS</sub> =10V		41.2		nC
Gate-Source Charge	Q <sub>gs</sub>			16.3		nC
Gate-Drain Charge	Q <sub>gd</sub>			12.8		nC
Gate plateau voltage	V <sub>gp</sub>			7.0		V
Intrinsic gate resistance	R <sub>G</sub>	f = 1 MHz open drain		1.5		Ω
Switching times						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =380V,I <sub>D</sub> =13A, R <sub>G</sub> =1.7Ω,V <sub>GS</sub> =10V		43		nS
Turn-on Rise Time	t <sub>r</sub>			16		nS
Turn-Off Delay Time	t <sub>d(off)</sub>			93		nS
Turn-Off Fall Time	t <sub>f</sub>			20		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I <sub>SD</sub>	T <sub>C</sub> =25℃			26	A
Pulsed Source-drain current(Body Diode)	I <sub>SDM</sub>				78	A
Forward On Voltage	V <sub>SD</sub>	T <sub>j</sub> =25℃,I <sub>SD</sub> =26A,V <sub>GS</sub> =0V		1.0	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>j</sub> =25℃,I <sub>F</sub> =13A,di/dt=100A/μs		145		nS
Reverse Recovery Charge	Q <sub>rr</sub>			0.725		uC
Peak Reverse Recovery Current	I <sub>rrm</sub>			10		A

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

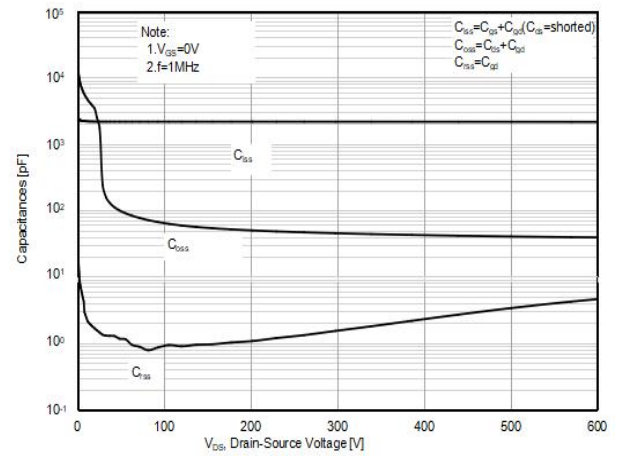
2.  $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

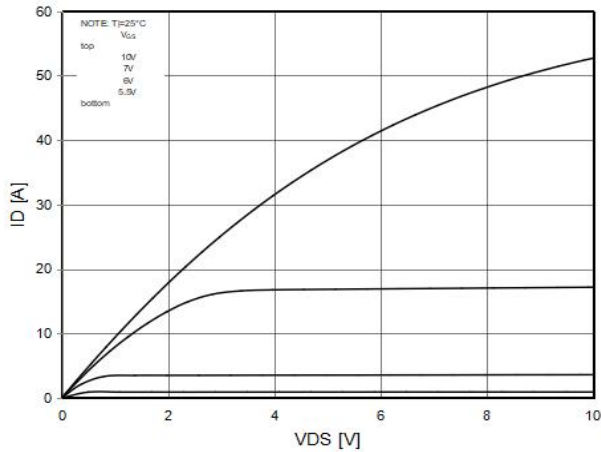
**Figure1. Safe operating area**



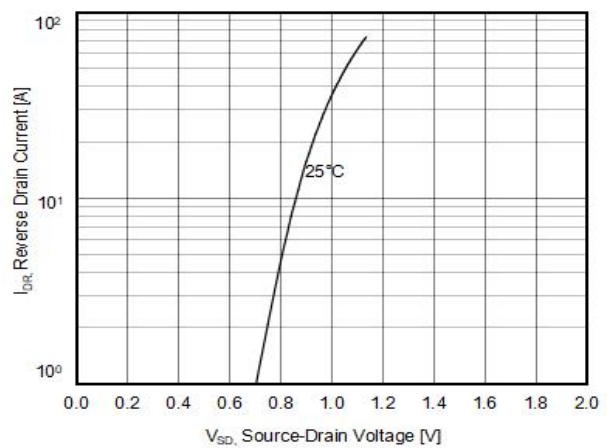
**Figure2. Capacitance**



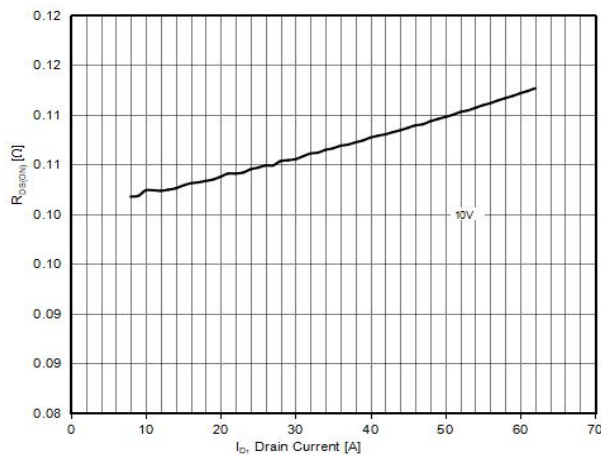
**Figure3. Output characteristics**



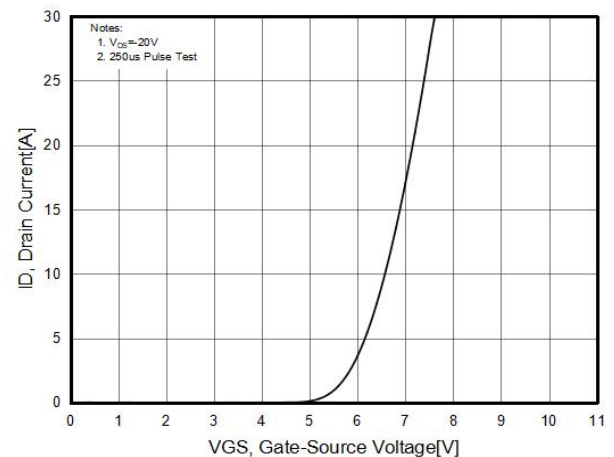
**Figure4. Source-Drain Diode Forward Voltage**



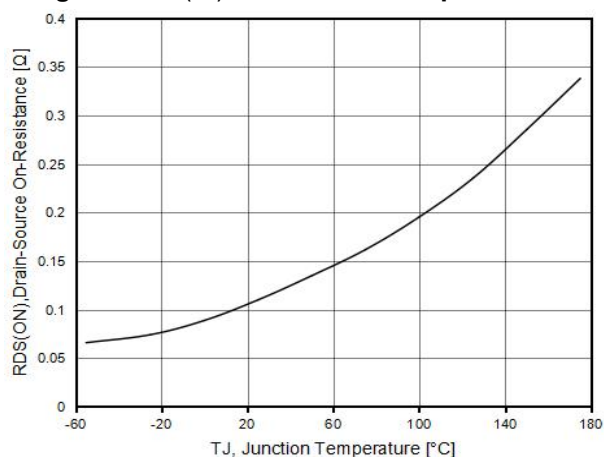
**Figure5. Static drain-source on resistance**



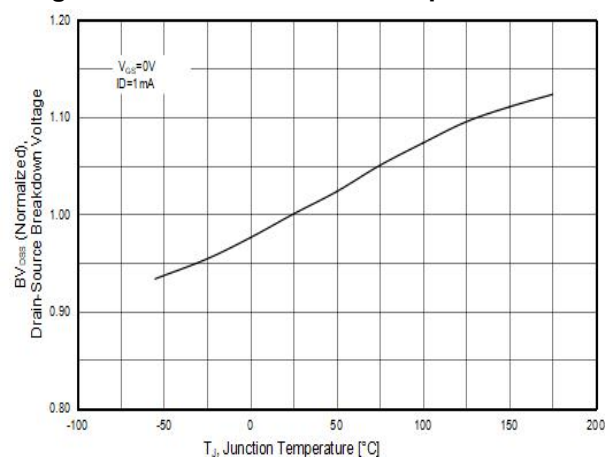
**Figure6. Transfer characteristics**



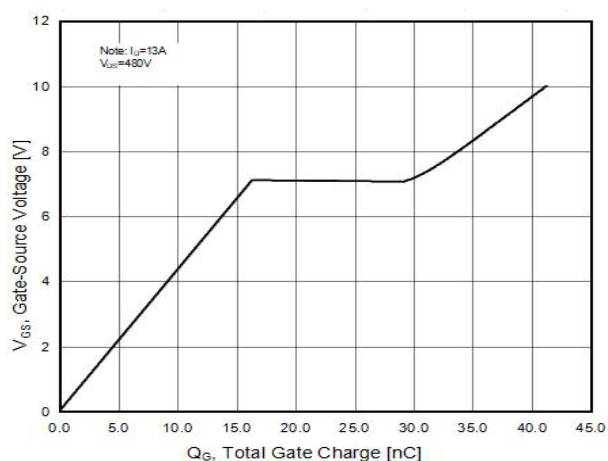
**Figure7.  $R_{DS(ON)}$  vs Junction Temperature**



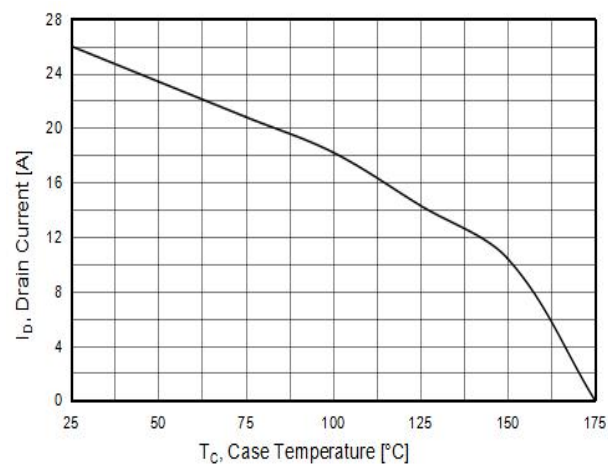
**Figure8.  $BV_{DSS}$  vs Junction Temperature**



**Figure9. Gate charge waveforms**

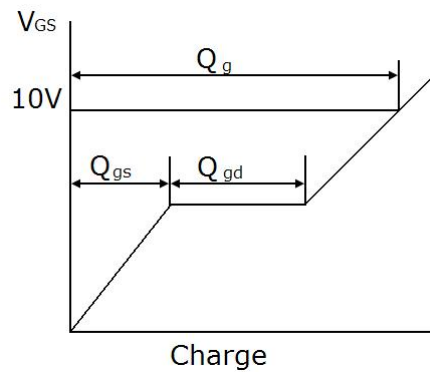
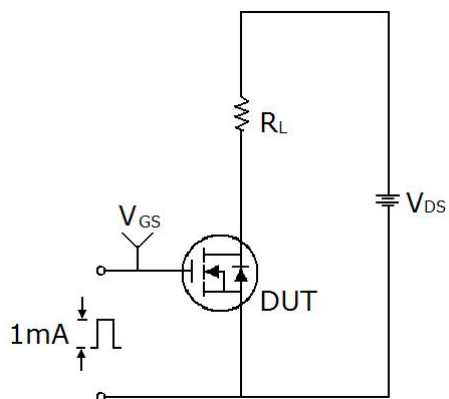


**Figure10. Maximum  $I_D$  vs Junction Temperature**

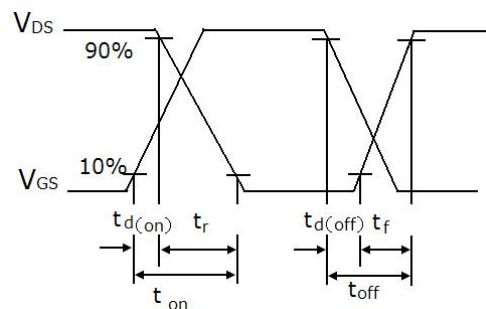
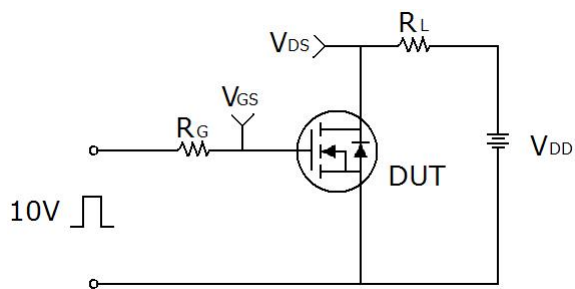


## Test circuit

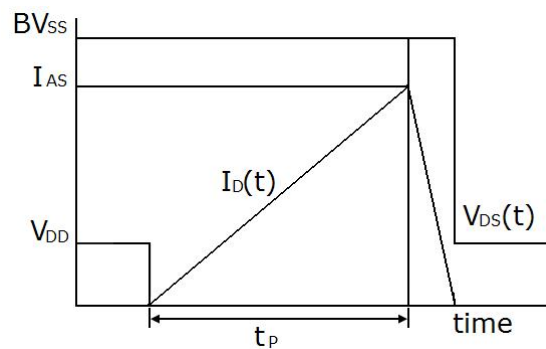
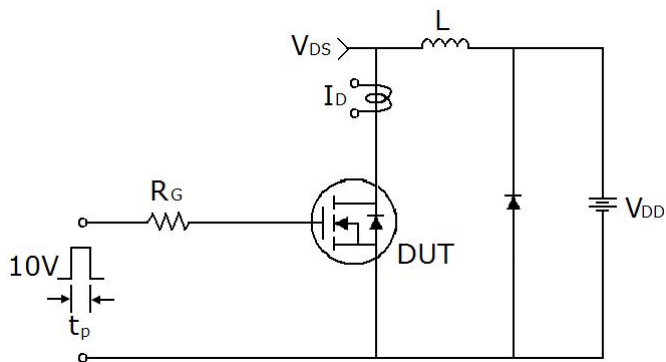
### 1) Gate charge test circuit & Waveform



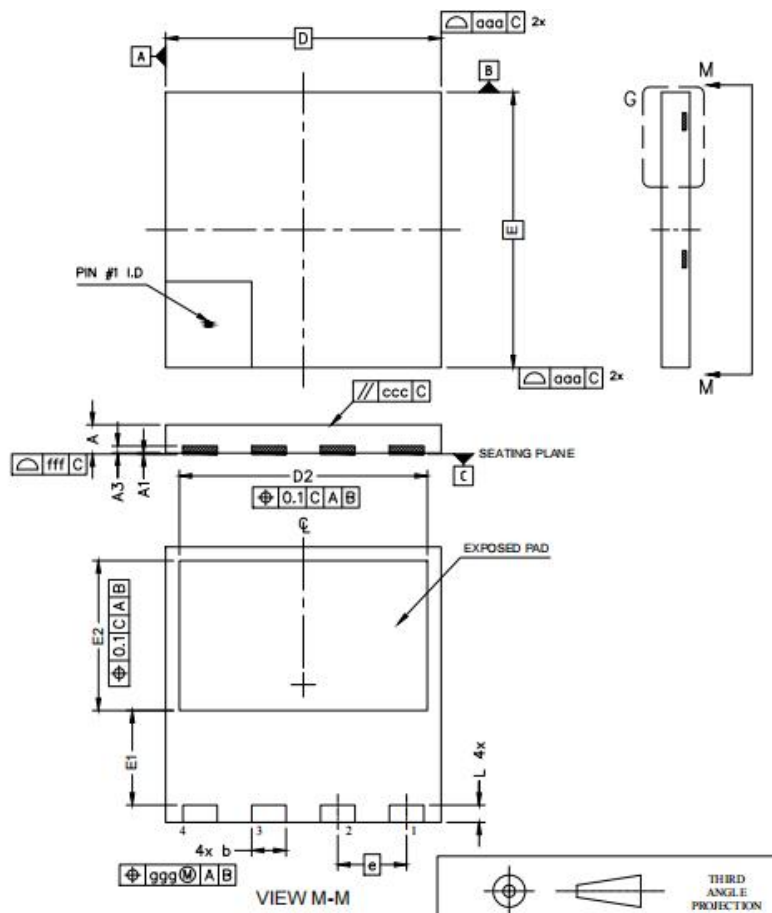
### 2) Switch Time Test Circuit:



### 3) Unclamped Inductive Switching Test Circuit & Waveforms



## DFN8\*8 (B) Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.75	0.95	0.030	0.037
A1	0.00	0.05	0.000	0.002
b	0.90	1.10	0.035	0.043
A3	0.10	0.30	0.004	0.012
D	7.90	8.10	0.311	0.319
E	7.90	8.10	0.311	0.319
D2	7.10	7.30	0.280	0.287
E1	2.65	2.85	0.104	0.112
E2	4.25	4.45	0.167	0.175
e	2.00 BSC		0.079 BSC	
L	0.40	0.60	0.016	0.024

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