

N-Channel Super Junction Power MOSFET IV

General Description

The series of devices use advanced trench gate super junction technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This super junction MOSFET fits the industry's AC-DC SMPS requirements for PFC, AC/DC power conversion, and industrial power applications.

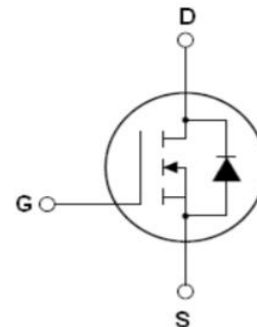
Features

- Optimized body diode reverse recovery performance
- Low on-resistance and low conduction losses
- Small package
- Ultra Low Gate Charge cause lower driving requirements
- 100% Avalanche Tested
- ROHS compliant

Application

- Power factor correction (PFC)
- Switched mode power supplies(SMPS)
- Uninterruptible Power Supply (UPS)
- LLC Half-bridge

$V_{DS \min @ T_{jmax}}$	750	V
$R_{DS(ON)TYP.}$	1000	m Ω
I_D	4.5	A
Q_g	9.5	nC



Schematic diagram

Package Marking And Ordering Information

Device	Device Package	Marking
NCE70N1K1F	TO-220F-3L	NCE70N1K1F



Table 1. Absolute Maximum Ratings ($T_c=25^\circ\text{C}$)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS}=0V$)	V_{DS}	700	V
Gate-Source Voltage ($V_{DS}=0V$), AC ($f>1\text{ Hz}$)	V_{GS}	± 30	V
Gate-Source Voltage ($V_{DS}=0V$), DC	V_{GS}	± 20	V
Continuous Drain Current at $T_c=25^\circ\text{C}$	$I_D (DC)$	4.5	A
Continuous Drain Current at $T_c=100^\circ\text{C}$	$I_D (DC)$	3.15	A
Pulsed drain current (Note 1)	$I_{DM} (pluse)$	13.5	A
Maximum Power Dissipation($T_c=25^\circ\text{C}$)	P_D	30.1	W
Derate above 25°C		0.20	W/ $^\circ\text{C}$
Single pulse avalanche current (Note 2)	I_{AS}	1.2	A
Reverse diode dv/dt , $V_{DS} \leq 480\text{ V}$, $I_{SD} < I_D$	dv/dt	15	V/ns
Drain Source voltage slope, $V_{DS} \leq 480\text{ V}$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	$-55...+175$	$^\circ\text{C}$

Table 2. Thermal Characteristic

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Maximum)	R_{thJC}	4.98	$^{\circ}\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient (Maximum)	R_{thJA}	62	$^{\circ}\text{C}/\text{W}$

Table 3. Electrical Characteristics (TA=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
On/off states						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250uA	700			V
Zero Gate Voltage Drain Current(Tc=25℃)	I _{DSS}	V _{DS} =700V,V _{GS} =0V			1	μA
Zero Gate Voltage Drain Current(Tc=125℃)	I _{DSS}	V _{DS} =700V,V _{GS} =0V			50	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V			±200	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250uA	3		4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =2.3A		1000	1100	mΩ
Dynamic Characteristics						
Gate Resistance	R _g	F=1MHZ, D-S short		36		Ω
Input Capacitance	C _{iss}	V _{DS} =50V,V _{GS} =0V, F=1MHz		311		pF
Output Capacitance	C _{oss}			14		pF
Reverse Transfer Capacitance	C _{rss}			4		pF
Total Gate Charge	Q _g	V _{DS} =500V,I _D =2.3A, V _{GS} =10V		9.5		nC
Gate-Source Charge	Q _{gs}			3		nC
Gate-Drain Charge	Q _{gd}			2.7		nC
Gate plateau voltage	V _{gp}			5.5		V
Switching times						
Turn-on Delay Time	t _{d(on)}	V _{DD} =500V,I _D =2.3A, R _G =4Ω,V _{GS} =10V		8		nS
Turn-on Rise Time	t _r			5		nS
Turn-Off Delay Time	t _{d(off)}			48		nS
Turn-Off Fall Time	t _f			8		nS
Source- Drain Diode Characteristics						
Source-drain current(Body Diode)	I _{SD}	T _C =25℃			4.5	A
Pulsed-Source-drain current(Body Diode)	I _{SDM}				13.5	A
Forward on voltage	V _{SD}	T _j =25℃,I _{SD} =4.5A,V _{GS} =0V		0.9	1.1	V
Reverse Recovery Time	t _{rr}	T _j =25℃,I _f 2.3A, di/dt=100A/μs		170		nS
Reverse Recovery Charge	Q _{rr}			0.46		uC
Peak reverse recovery current	I _{rrm}			5.5		A

Notes: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. $T_j=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, R_G=25\Omega$

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (curves)

Figure1. Safe operating area

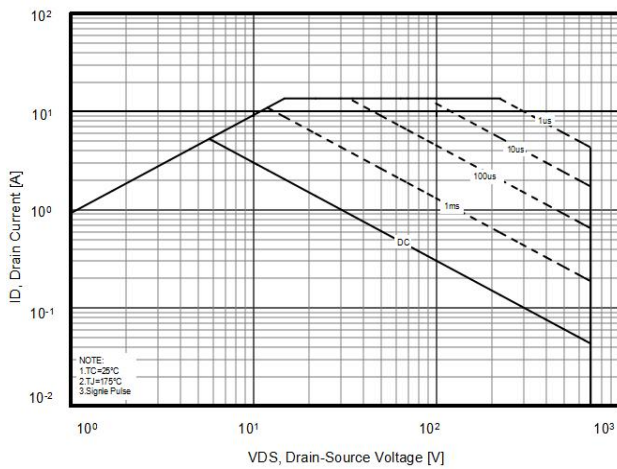


Figure2. Source-Drain Diode Forward Voltage

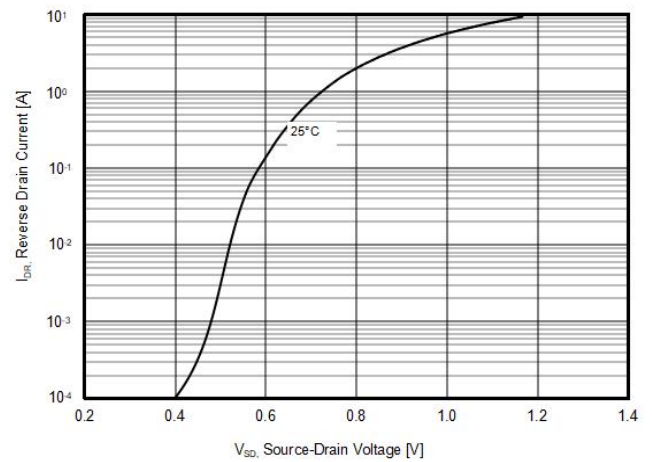


Figure3. Output characteristics

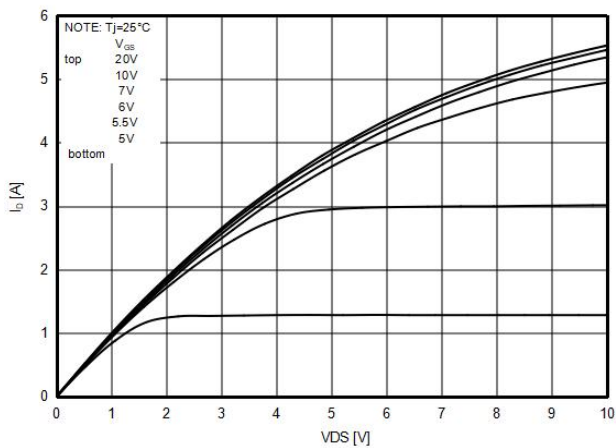


Figure4. Transfer characteristics

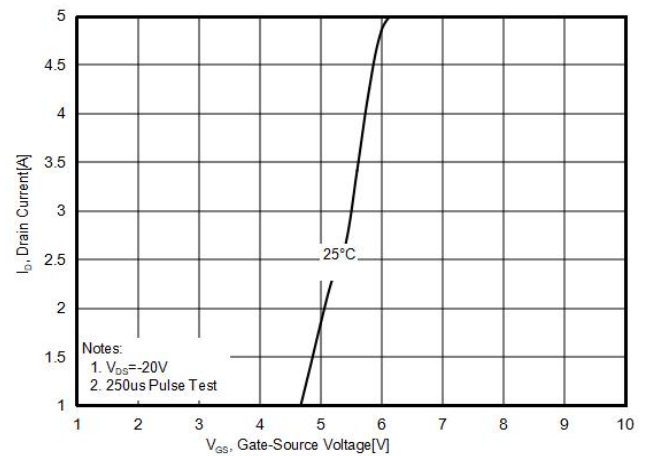


Figure5. Static drain-source on resistance

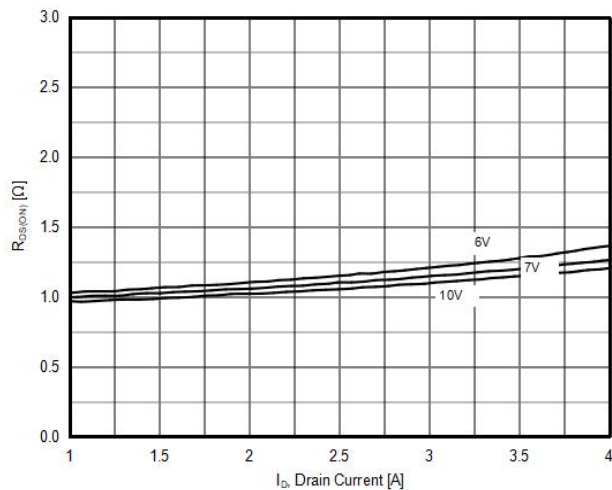


Figure6. $R_{DS(on)}$ vs Junction Temperature

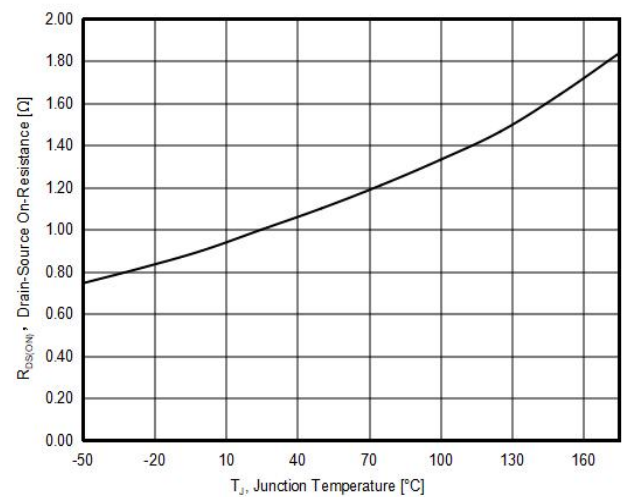


Figure7. BV_{DS} vs Junction Temperature

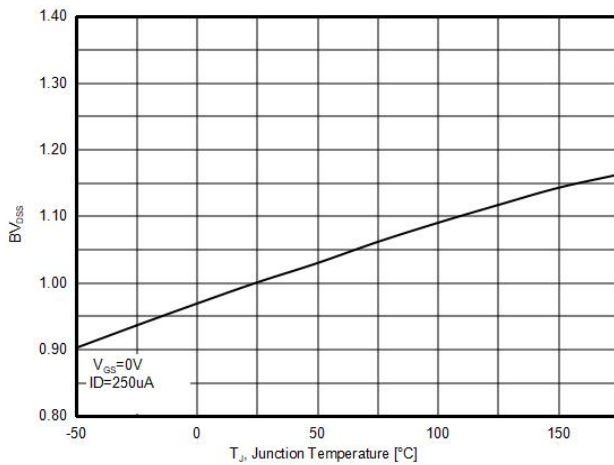


Figure8. Maximum I_D vs Junction Temperature

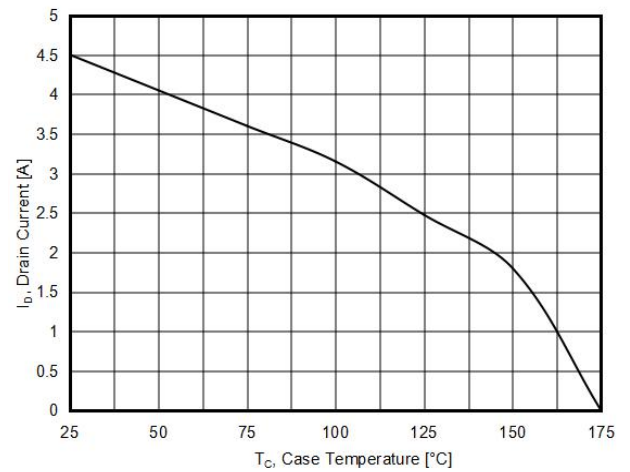


Figure9. Gate charge waveforms

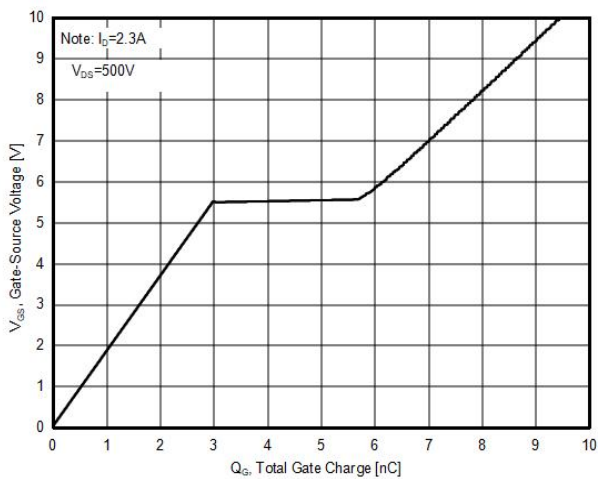
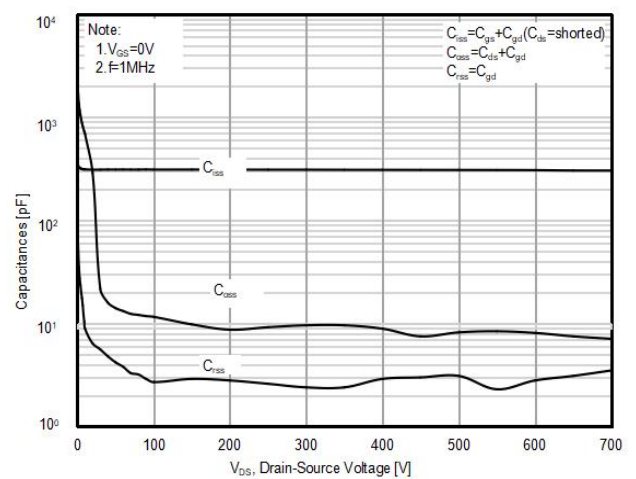
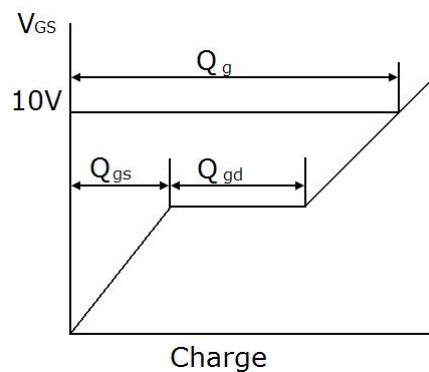


Figure10. Capacitance

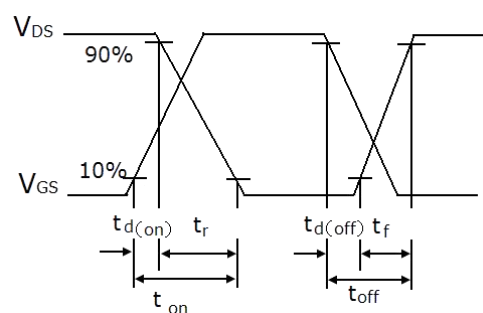
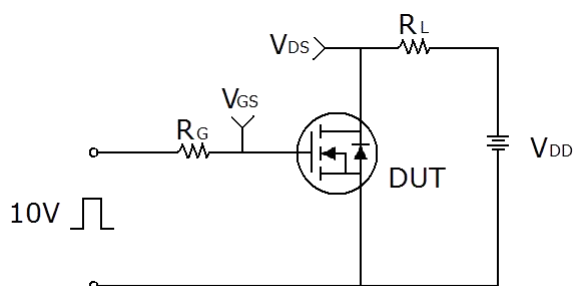


Test circuit

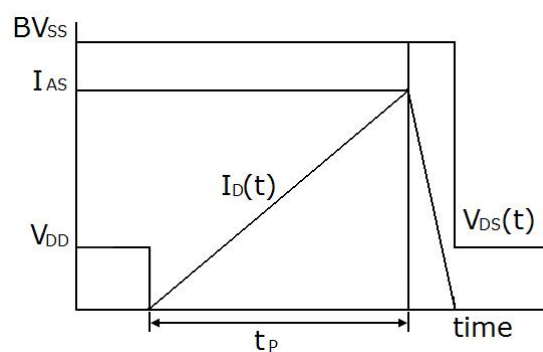
1) Gate charge test circuit & Waveform



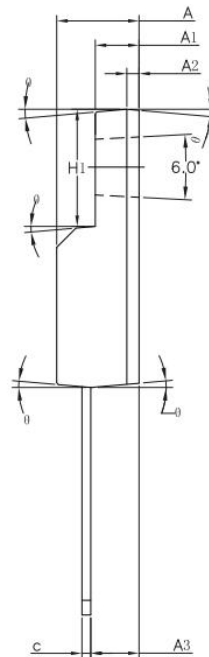
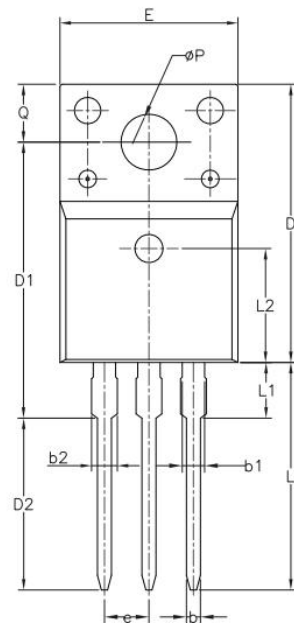
2) Switch Time Test Circuit:



3) Unclamped Inductive Switching Test Circuit & Waveforms



TO-220F-P Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.50	4.83	0.177	0.190
A1	2.34	2.74	0.092	0.108
A2	0.70 REF		0.028 REF	
A3	2.56	2.93	0.101	0.115
b	0.70	0.90	0.028	0.035
b1	1.18	1.38	0.046	0.054
b2	--	1.47	--	0.058
c	0.45	0.60	0.018	0.024
D	15.67	16.07	0.616	0.631
D1	15.55	15.95	0.611	0.627
D2	9.60	10.00	0.377	0.393
E	9.96	10.36	0.391	0.407
e	2.54 BSC		0.100 BSC	
H1	6.48	6.88	0.255	0.270
L	12.68	13.28	0.498	0.522
L1	--	3.50	--	0.138
L2	6.50 REF		0.255 REF	
Ø P	3.08	3.28	0.121	0.129
Q	3.20	3.40	0.126	0.134
θ1	1.0°	5.0°	1.00°	5.00°

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