

## NCE P-Channel Enhancement Mode Power MOSFET

### Description

The NCEA01P35G uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### Application

- Automotive application
- Portable equipment and battery powered systems

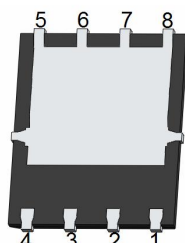
### General Features

- $V_{DS} = -100V, I_D = -35A$
- $R_{DS(ON)} < 40m\Omega @ V_{GS} = -10V$  (Typ: 30m $\Omega$ )
- $R_{DS(ON)} < 45m\Omega @ V_{GS} = -4.5V$  (Typ: 32m $\Omega$ )
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance
- 175 °C operating temperature
- 100% UIS tested
- 100%  $\Delta V_{ds}$  tested
- **AEC-Q101 qualified**

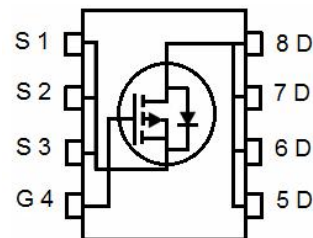
### PDFN 5X6-8L



Top View



Bottom View



Schematic Diagram

### Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
A01P35G	NCEA01P35G	PDFN5X6-8L	Ø330mm	12mm	5000units

### Absolute Maximum Ratings ( $T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	-100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	-35	A
Drain Current-Continuous( $T_c = 100^\circ C$ )	$I_D (100^\circ C)$	-26	A
Pulsed Drain Current	$I_{DM}$	-140	A
Maximum Power Dissipation	$P_D$	120	W
Single pulse avalanche energy (Note 1)	$E_{AS}$	145.8	mJ
Derating factor		0.8	W/ $^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

## Thermal Characteristic

Thermal Resistance,Junction-to-Case	$R_{\theta JC}$	1.25	$^{\circ}\text{C/W}$
Thermal Resistance,Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	$^{\circ}\text{C/W}$

## Electrical Characteristics ( $T_C=25^{\circ}\text{C}$ unless otherwise noted)

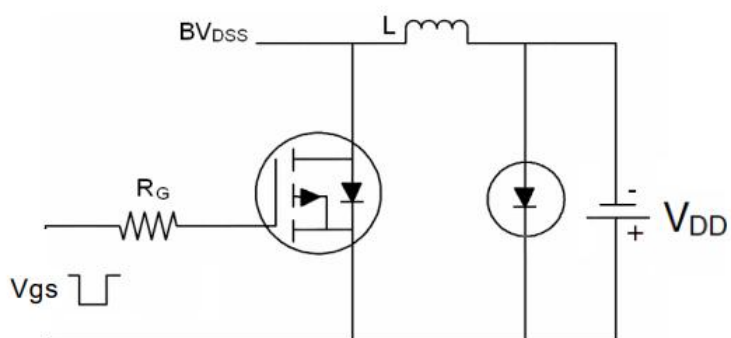
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-100	-	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-100V, V <sub>GS</sub> =0V	-	-	1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1.3	-1.8	-2.5	V
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A	-	30	40	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A	-	32	45	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-20A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-50V, V <sub>GS</sub> =0V, F=1.0MHz	-	5720	-	pF
Output Capacitance	C <sub>Oss</sub>		-	190	-	pF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	128	-	pF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-50V, I <sub>D</sub> =-20A V <sub>GS</sub> =-10V, R <sub>GEN</sub> =9.1Ω	-	17	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	80	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	45	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	65	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-50V, I <sub>D</sub> =-20A, V <sub>GS</sub> =-10V	-	118	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	19.8	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	22.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-20A	-	-	-1.2	V
Diode Forward Current	I <sub>S</sub>	-	-	-	-35	A
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25°C, I <sub>F</sub> =-20A di/dt = 100A/μs	-	90	-	nS
Reverse Recovery Charge	Q <sub>rr</sub>		-	145	-	nC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

### Notes:

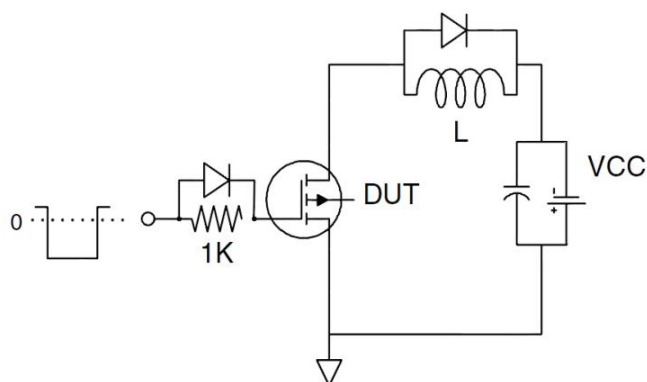
1. EAS condition :  $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, L=0.5mH, R_g=25\Omega$
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of  $T_{J(MAX)}=175^{\circ}\text{C}$ . The SOA curve provides a single pulse rating.
4. The value of  $R_{\theta JA}$  is measured with the device mounted on 1in<sup>2</sup> FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The maximum allowed junction temperature of  $175^{\circ}\text{C}$ . The value in any given application depends on the user's specific board design.

## Test Circuit

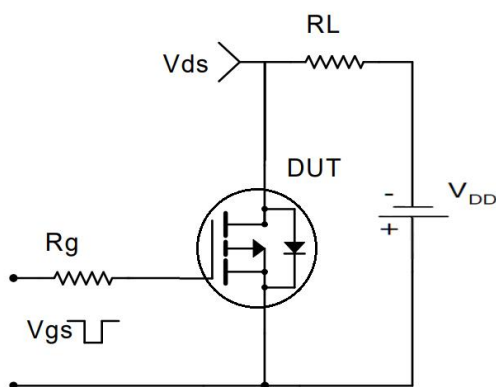
### 1) $E_{AS}$ test Circuit



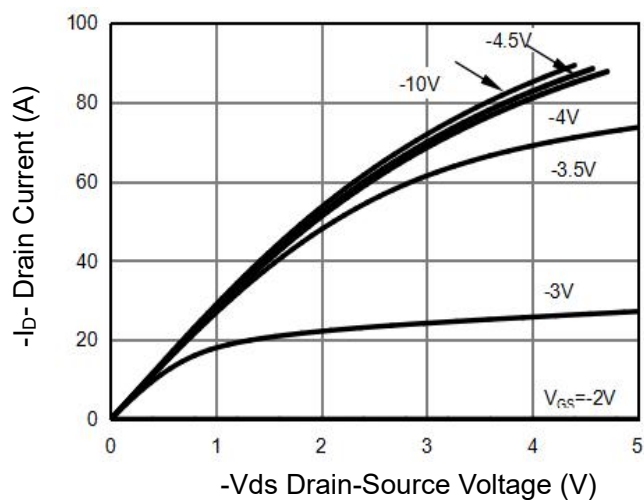
### 2) Gate charge test Circuit



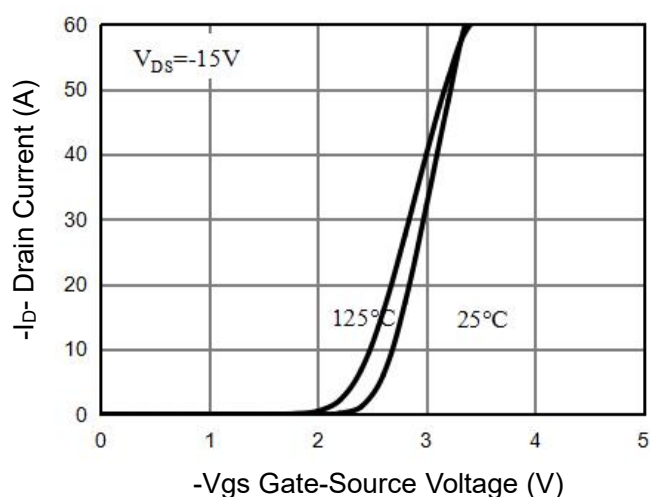
### 3) Switch Time Test Circuit



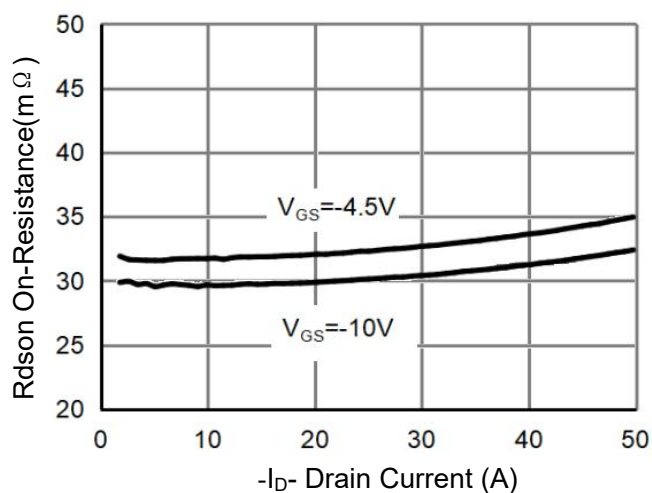
## Typical Electrical and Thermal Characteristics (Curves)



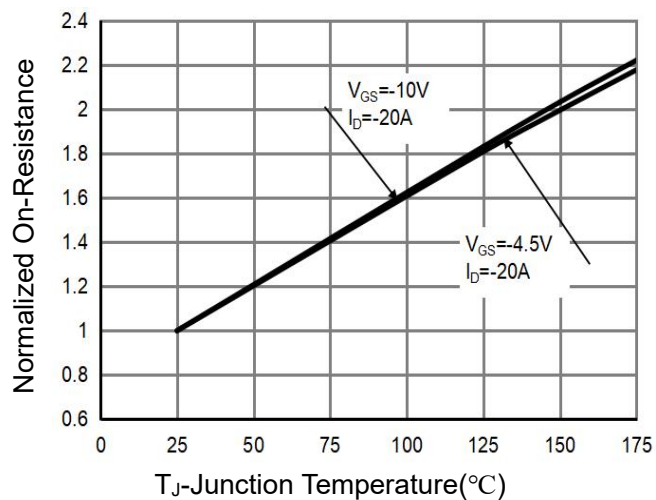
**Figure 1 Output Characteristics**



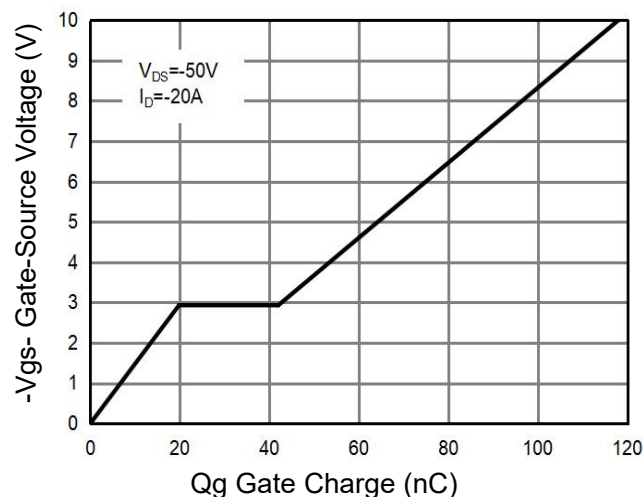
**Figure 2 Transfer Characteristics**



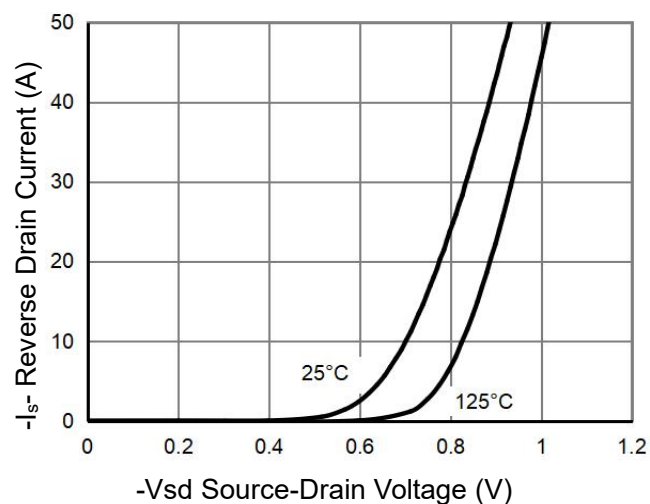
**Figure 3 Rdson- Drain Current**



**Figure 4 Rdson-Junction Temperature**



**Figure 5 Gate Charge**



**Figure 6 Source- Drain Diode Forward**

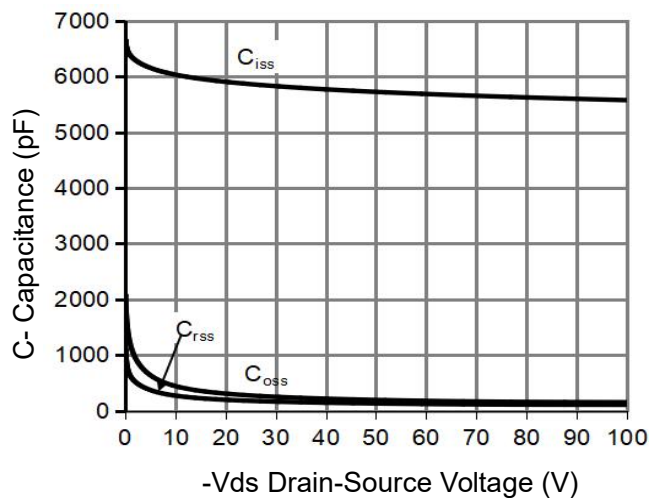


Figure 7 Capacitance vs Vds

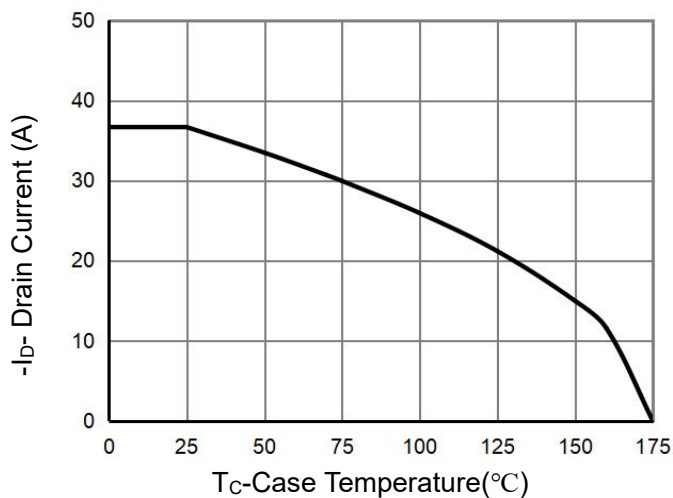


Figure 9 Drain Current vs Case Temperature

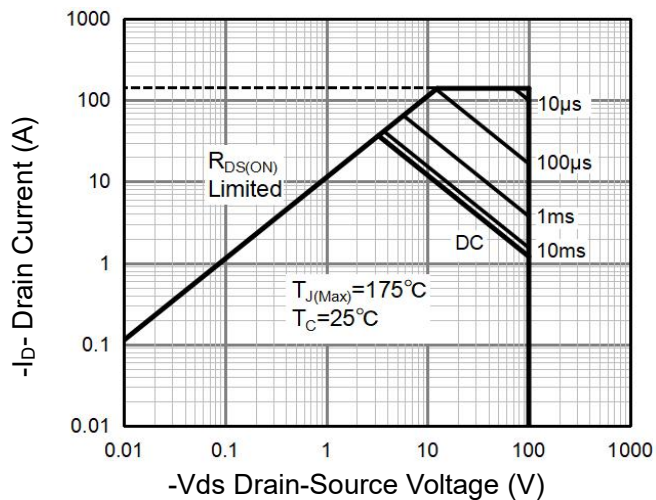


Figure 8 Safe Operation Area (Note3)

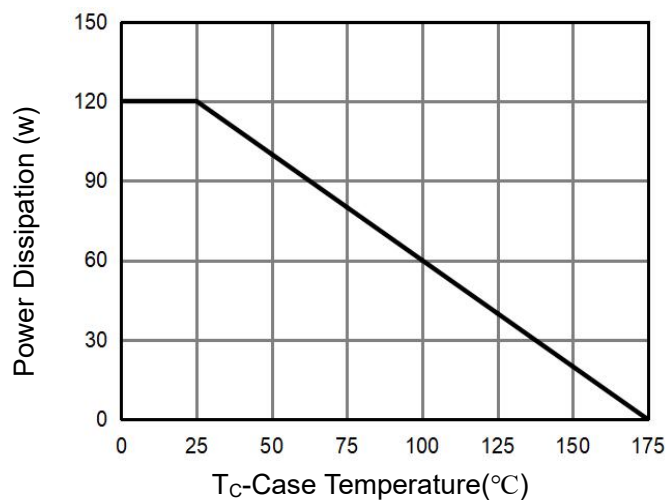


Figure 10 Power De-rating

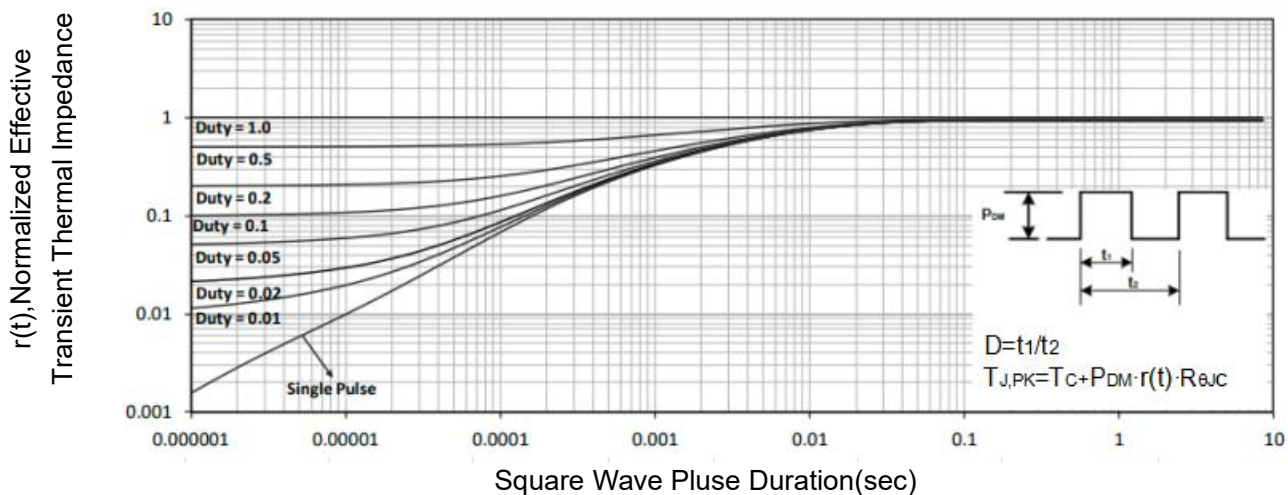
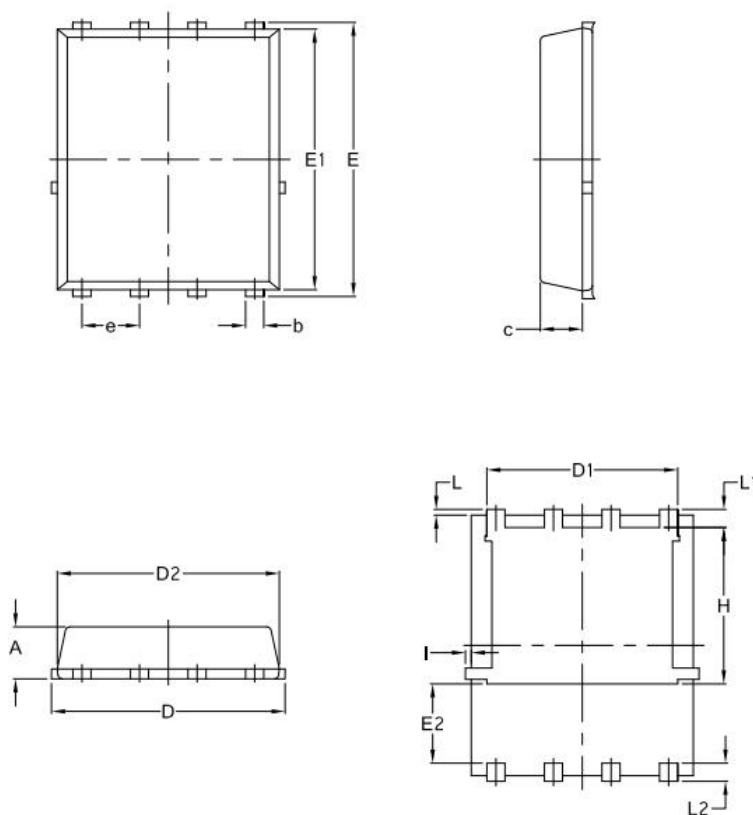


Figure 11 Normalized Maximum Transient Thermal Impedance

## PDFN5X6-8L Package Information



SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.970	0.0324	0.0382
△ D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
△ D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	—	0.0630	—
e	1.27 BSC		0.05 BSC	
△ L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
△ H	3.30	3.50	0.1299	0.1378
I	—	0.18	—	0.0070

## Revision History

Revision	Date	Subjects
V1.0	2025.08.11	Product data sheet

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