

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP0116K uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

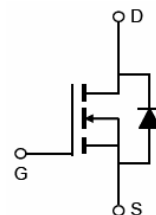
General Features

- $V_{DS} = 100V, I_D = 16A$
 $R_{DS(on)} = 78m\Omega$ (typical) @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- LED backlighting
- Ideal for high-frequency switching and synchronous rectification

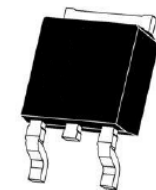
100% UIS TESTED!



Schematic diagram



Marking and pin assignment



TO-252 -2Ltop view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP0116K	NCEP0116K	TO-252-2L	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	16	A
Drain Current-Continuous($T_C = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	11.3	A
Pulsed Drain Current	I_{DM}	64	A
Maximum Power Dissipation	P_D	55	W
Derating factor		0.37	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	26	mJ
Drain Source voltage slope, $V_{DS} \leq 120\text{ V}$,	dv/dt	50	V/ns
Drain Source voltage slope, $V_{DS} \leq 120\text{ V}$, $I_{SD} < I_D$	dv/dt	50	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	°C

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.7	$^{\circ}\text{C/W}$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

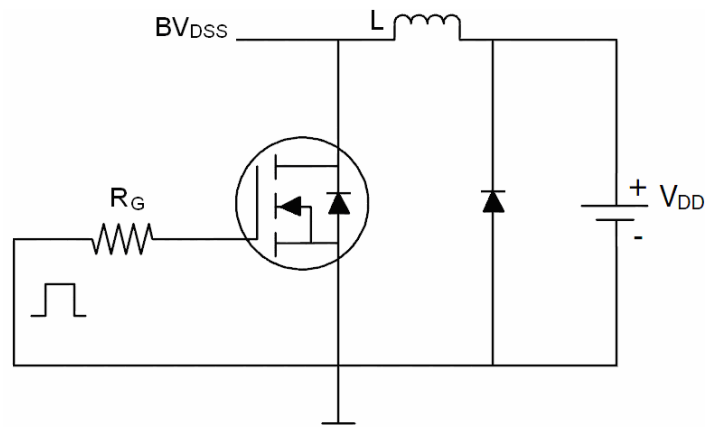
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.2	4.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=16A$	-	78	95	m Ω
Gate resistance	R_G		-	10	-	Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=16A$	-	20	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{iss}	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0MHz$	-	322		PF
Output Capacitance	C_{oss}		-	53		PF
Reverse Transfer Capacitance	C_{rss}		-	5.1		PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, R_L=3\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	6	-	nS
Turn-on Rise Time	t_r		-	3	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	18	-	nS
Turn-Off Fall Time	t_f		-	3	-	nS
Total Gate Charge	Q_g	$V_{DS}=50V, I_D=10A,$ $V_{GS}=10V$	-	5.6	-	nC
Gate-Source Charge	Q_{gs}		-	2.4	-	nC
Gate-Drain Charge	Q_{gd}		-	1.3	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	16	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = I_S$ $di/dt = 100A/\mu s$ (Note3)	-	15	-	nS
Reverse Recovery Charge	Q_{rr}		-	53	-	nC

Notes:

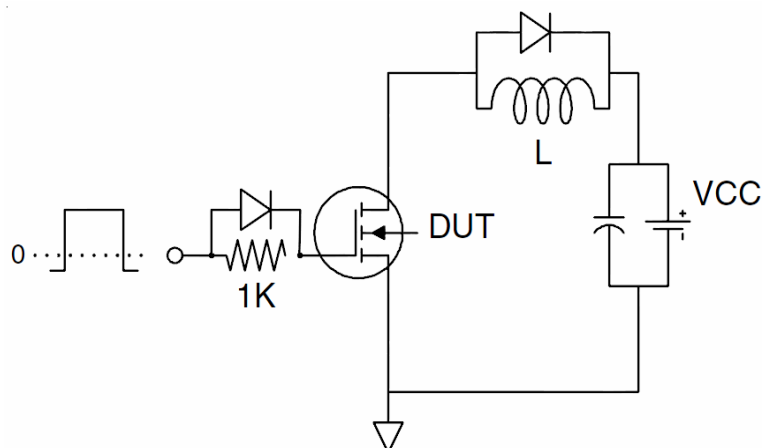
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

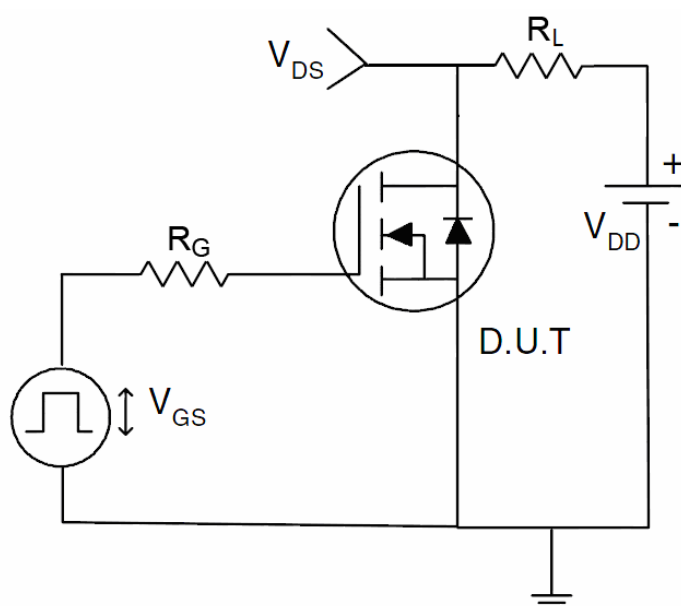
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

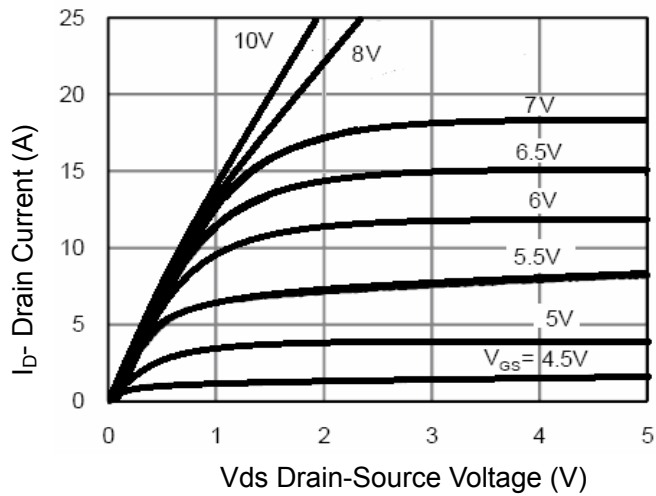


Figure 1 Output Characteristics

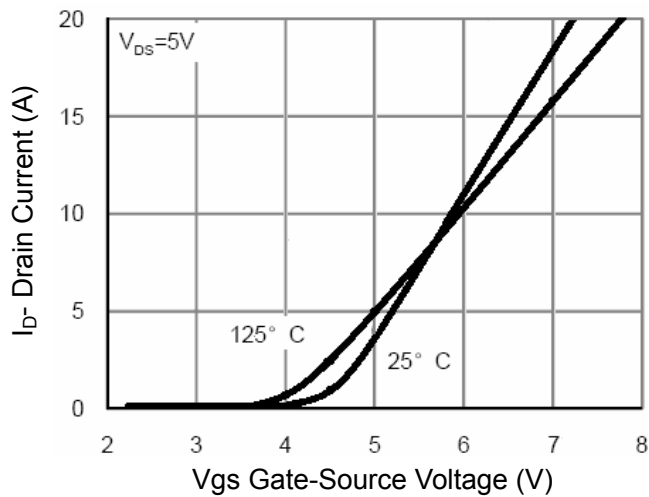


Figure 2 Transfer Characteristics

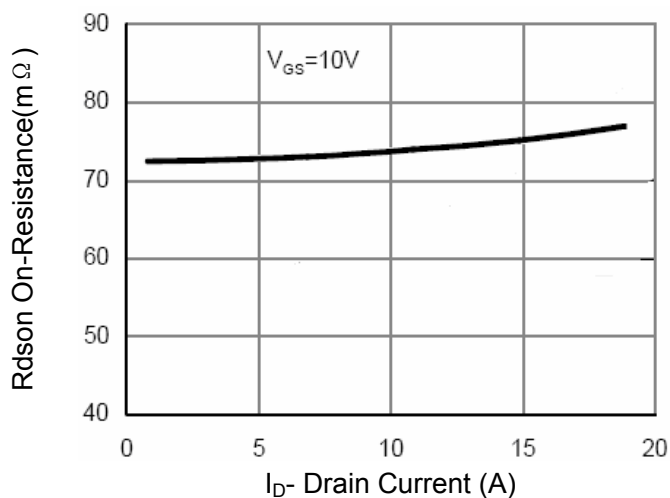


Figure 3 $R_{DS(on)}$ - Drain Current

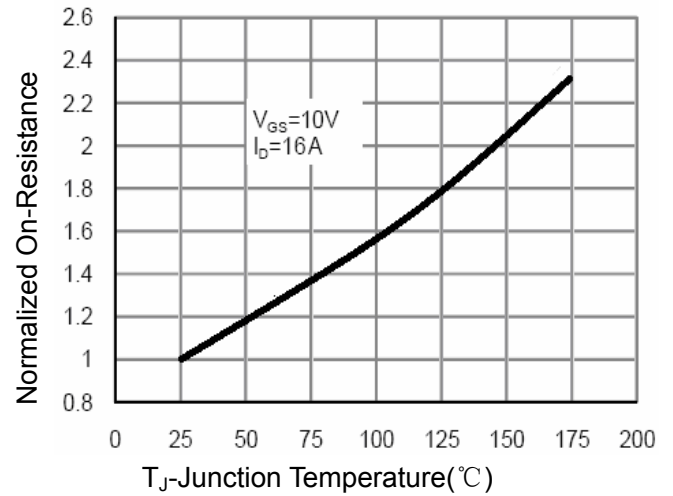


Figure 4 $R_{DS(on)}$ -Junction Temperature

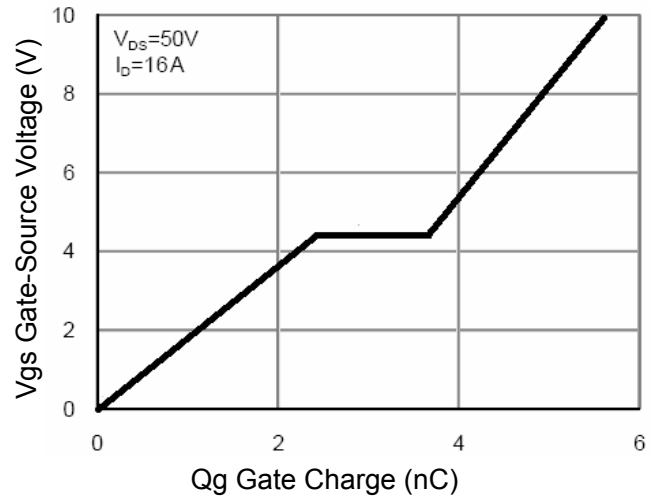


Figure 5 Gate Charge

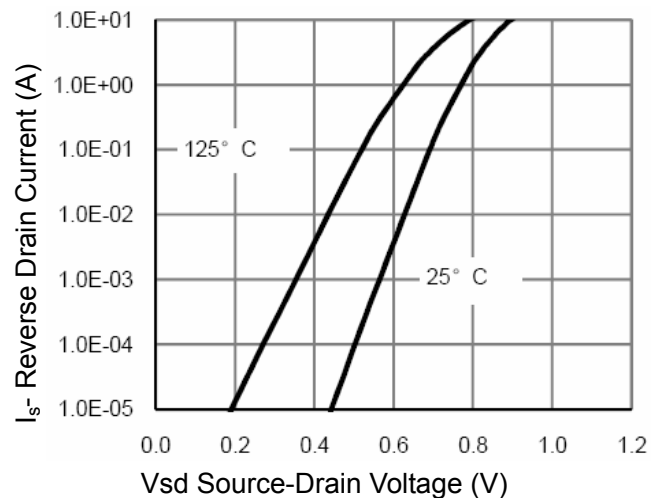


Figure 6 Source- Drain Diode Forward

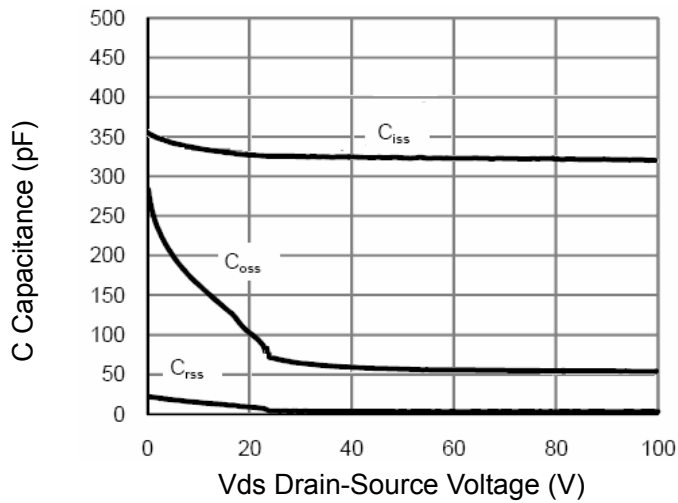


Figure 7 Capacitance vs Vds

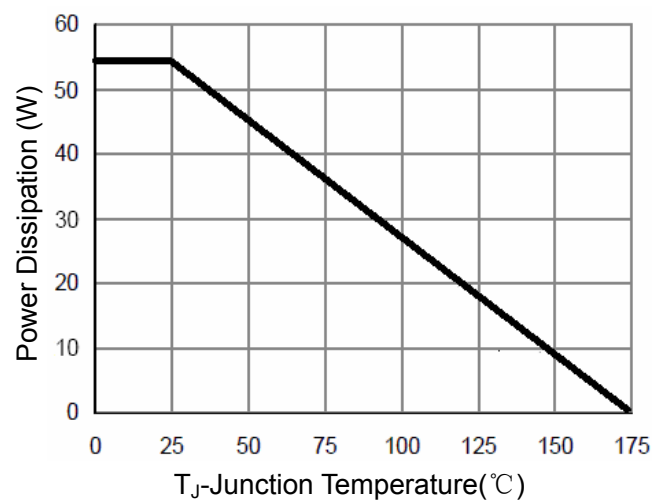


Figure 9 Power De-rating

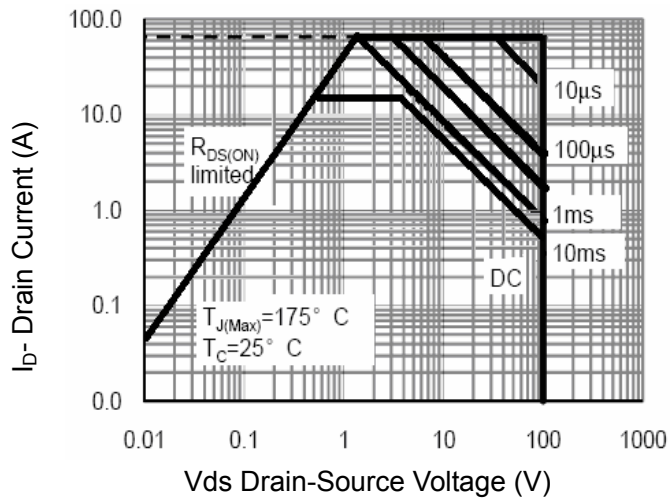


Figure 8 Safe Operation Area

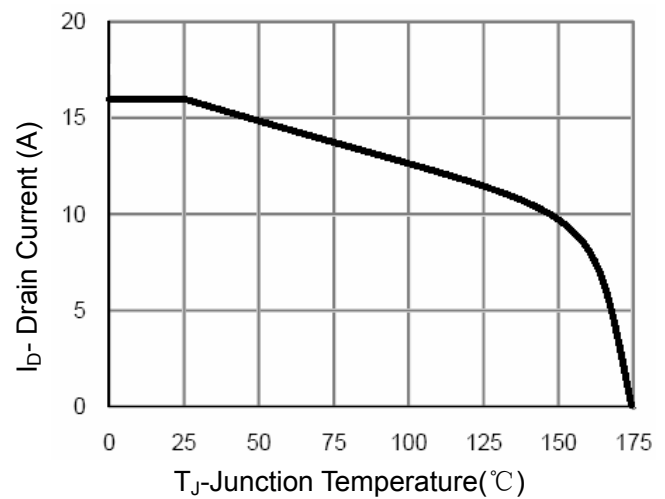


Figure 10 Current De-rating

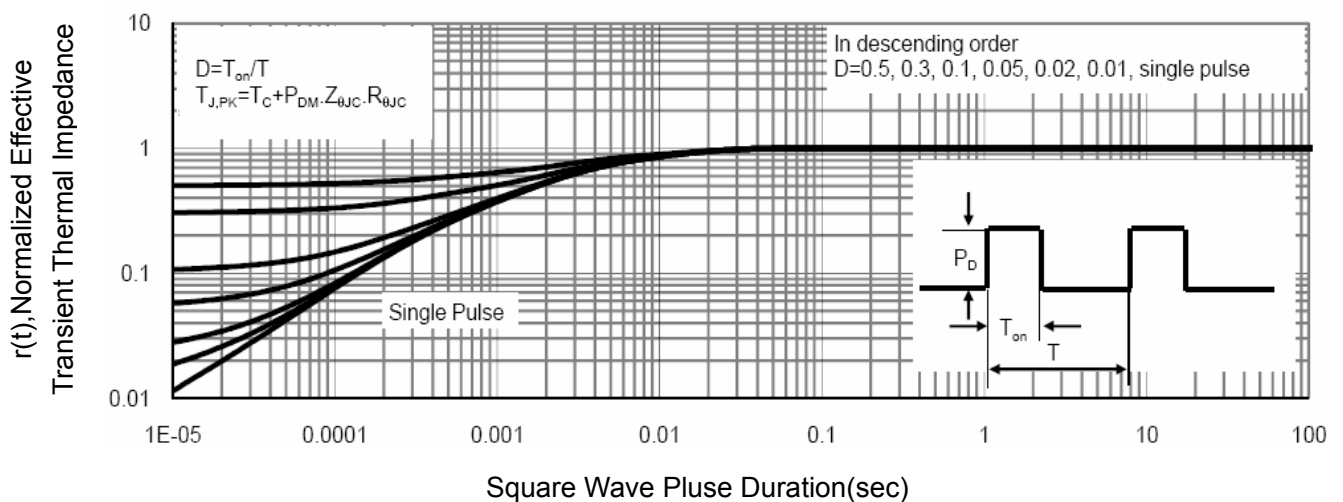


Figure 11 Normalized Maximum Transient Thermal Impedance

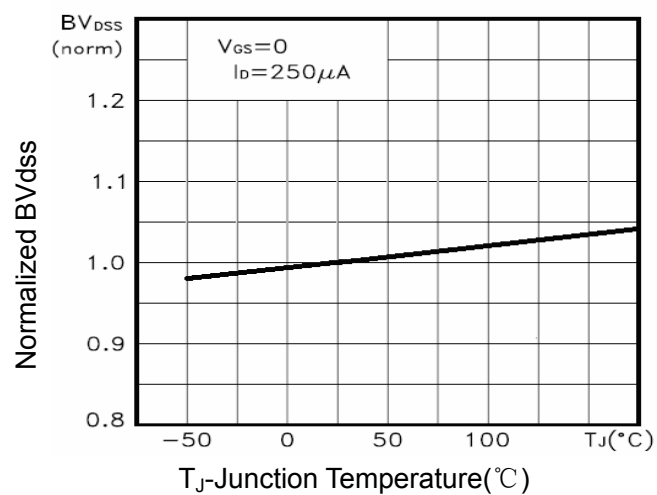
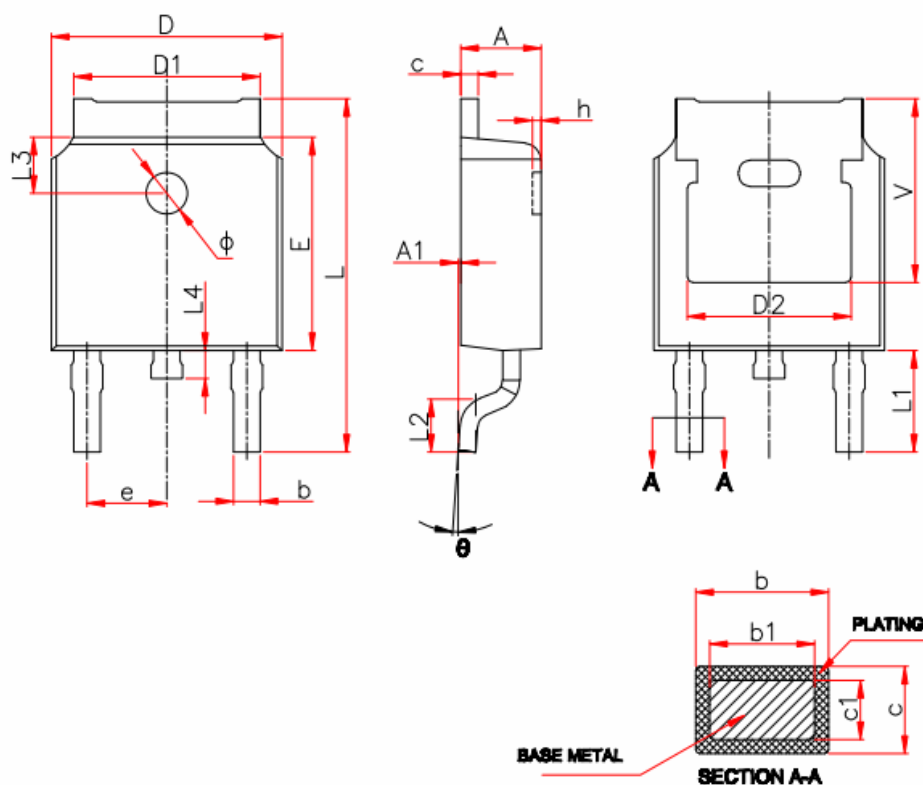


Figure 12 BV_{DSS} vs Junction Temperature

TO-252 Package Information


Symbol	Millimeters	
	Min.	Max.
A	2.20	2.40
A1	0.00	0.13
b	0.66	0.86
b1	0.73	0.79
c	0.46	0.58
c1	0.50	0.52
D	6.50	6.70
D1	5.10	5.46
D2	4.83 REF.	
E	6.00	6.20
e	2.19	2.39
L	9.80	10.40
L1	2.90 REF.	
L2	1.40	1.70
L3	1.60 REF.	
L4	0.60	1.00
ϕ	1.10	1.30
θ	0°	8°

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