

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP018N60AGU uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(on)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 60V, I_D = 195A$
 $R_{DS(on)} = 1.4 m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(on)} = 1.8 m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

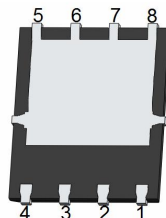
100% UIS TESTED!

100% ΔV_{ds} TESTED!

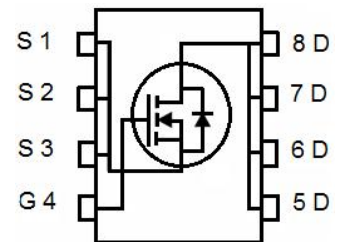
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P018N60AGU	NCEP018N60AGU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	195	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	135	A
Pulsed Drain Current	I_{DM}	780	A
Maximum Power Dissipation	P_D	220	W
Derating factor		1.76	W/ $^\circ C$
Single pulse avalanche energy (Note 1)	E_{AS}	871	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.57	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient (Note 4)	$R_{\theta JA}$	50	$^\circ C/W$

Electrical Characteristics (T_c=25°C unless otherwise noted)

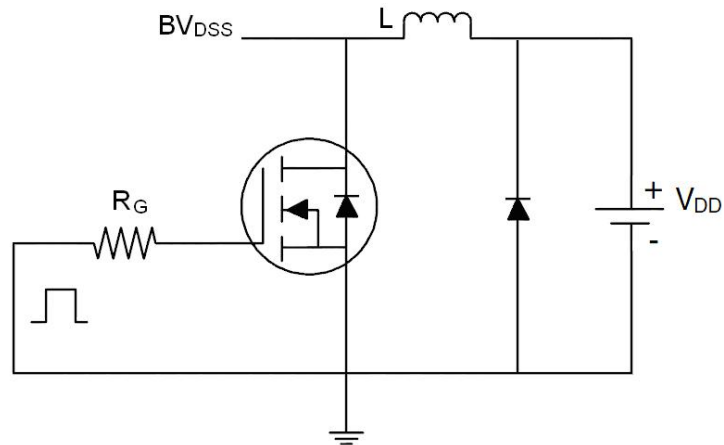
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	1.4	1.8	mΩ
		V _{GS} =4.5V, I _D =20A	-	1.8	2.4	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =20A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	6150	-	PF
Output Capacitance	C _{oss}		-	965	-	PF
Reverse Transfer Capacitance	C _{rss}		-	65	-	PF
Switching Characteristics <small>(Note 2)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =20A V _{GS} =10V, R _G =4.7Ω	-	17	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	60	-	nS
Turn-Off Fall Time	t _f		-	18	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =20A, V _{GS} =10V	-	103		nC
Gate-Source Charge	Q _{gs}		-	18		nC
Gate-Drain Charge	Q _{gd}		-	15.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =20A	-		1.2	V
Diode Forward Current	I _S		-	-	195	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S	-	60		nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs	-	85		nC

Notes:

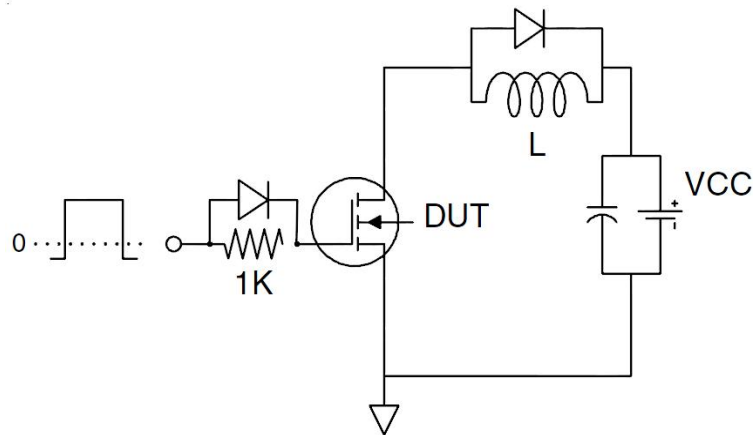
1. EAS condition : T_J=25°C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=150°C. The SOA curve provides a single pulse rating.
4. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

Test Circuit

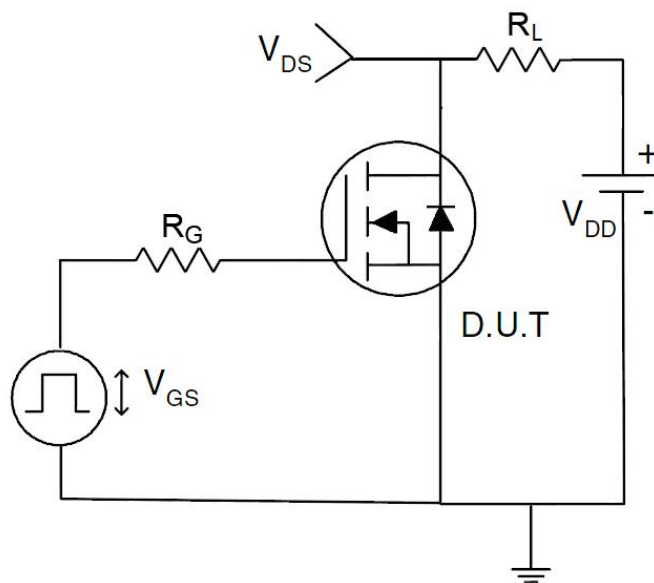
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

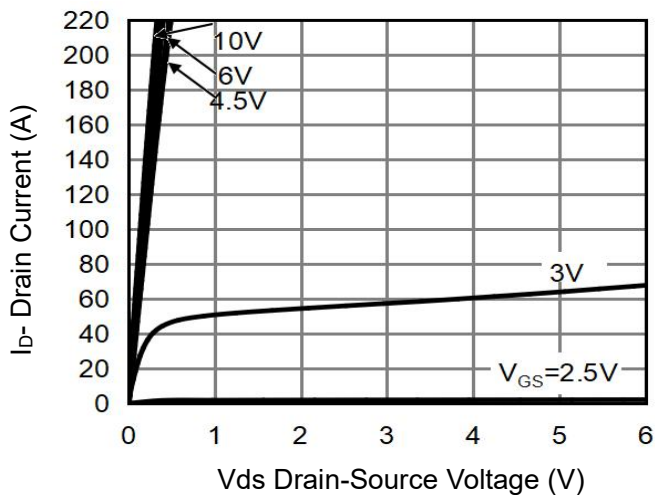


Figure 1 Output Characteristics

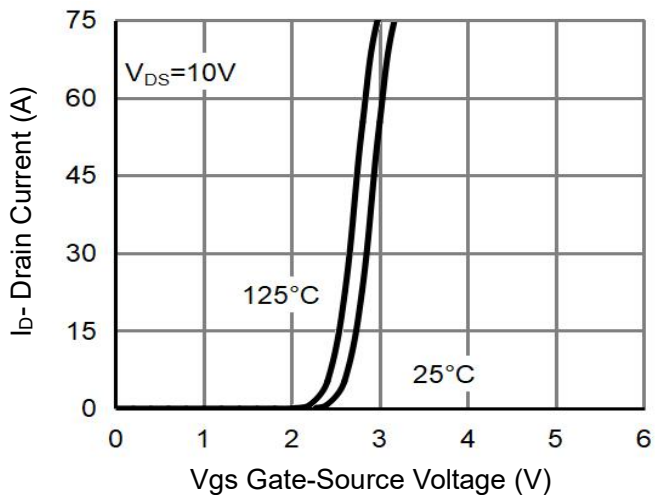


Figure 2 Transfer Characteristics

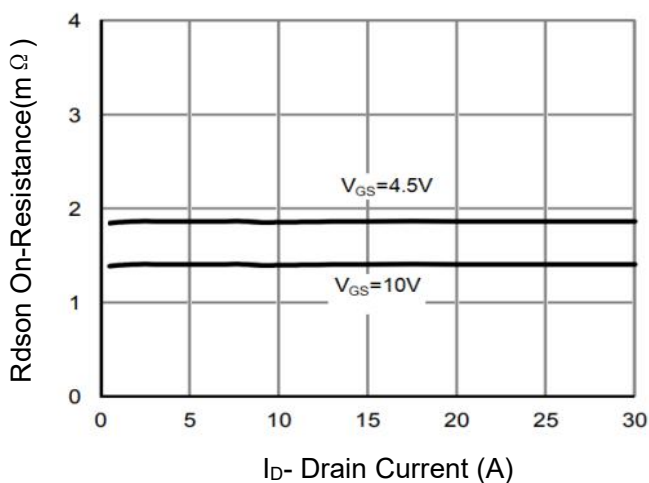


Figure 3 Rdson- Drain Current

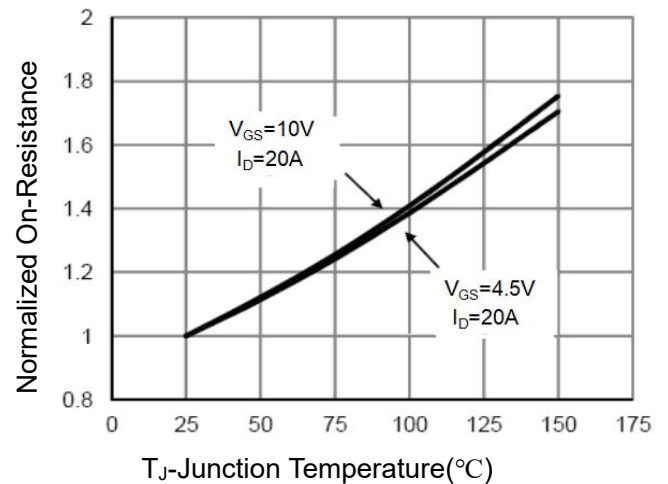


Figure 4 Rdson-Junction Temperature

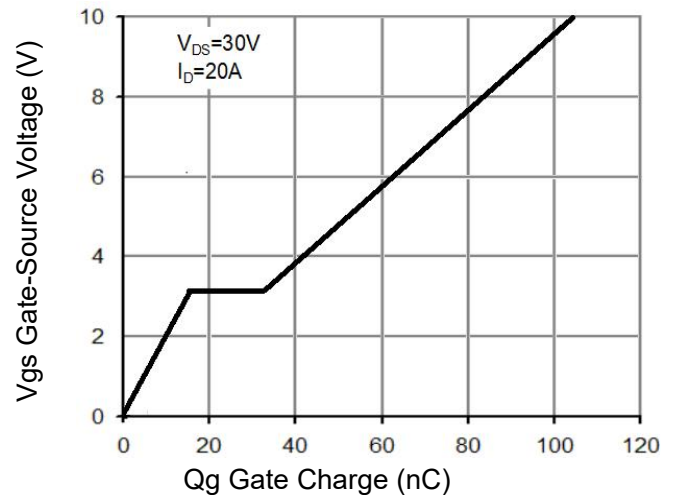


Figure 5 Gate Charge

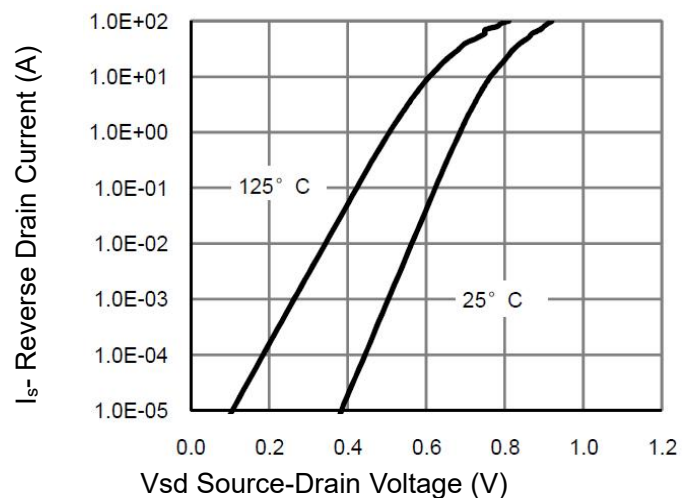


Figure 6 Source- Drain Diode Forward

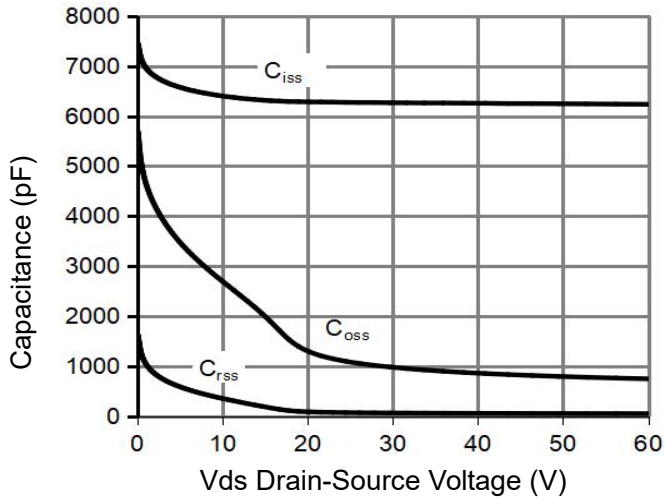


Figure 7 Capacitance vs Vds

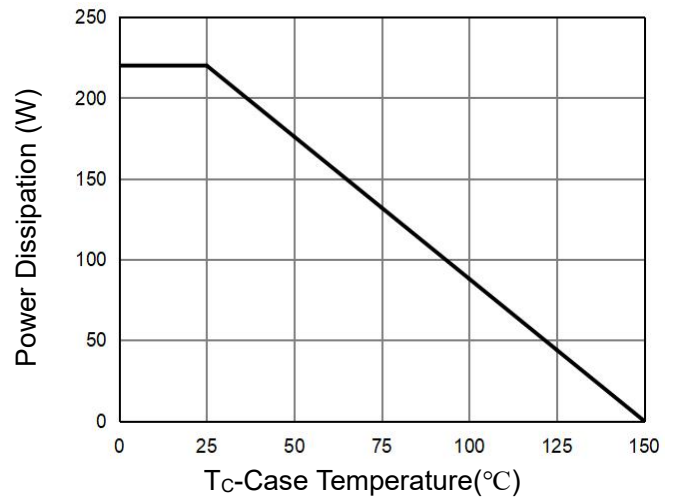


Figure 9 Power De-rating

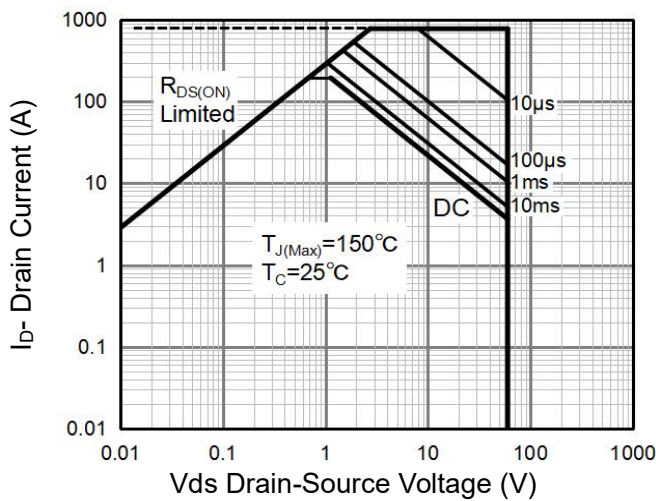


Figure 8 Safe Operation Area (Note 3)

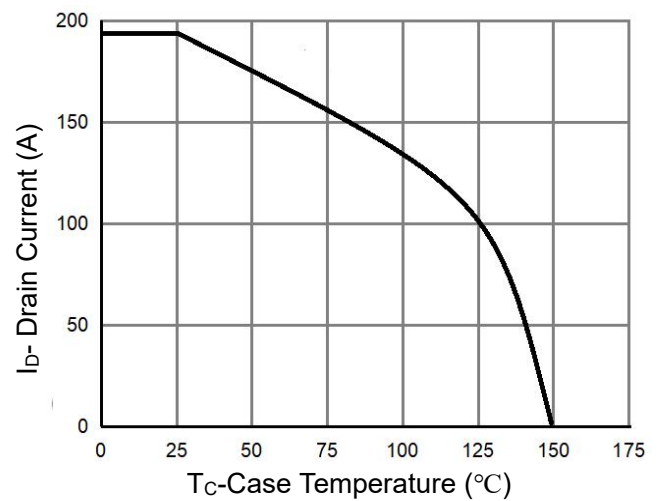


Figure 10 Current De-rating

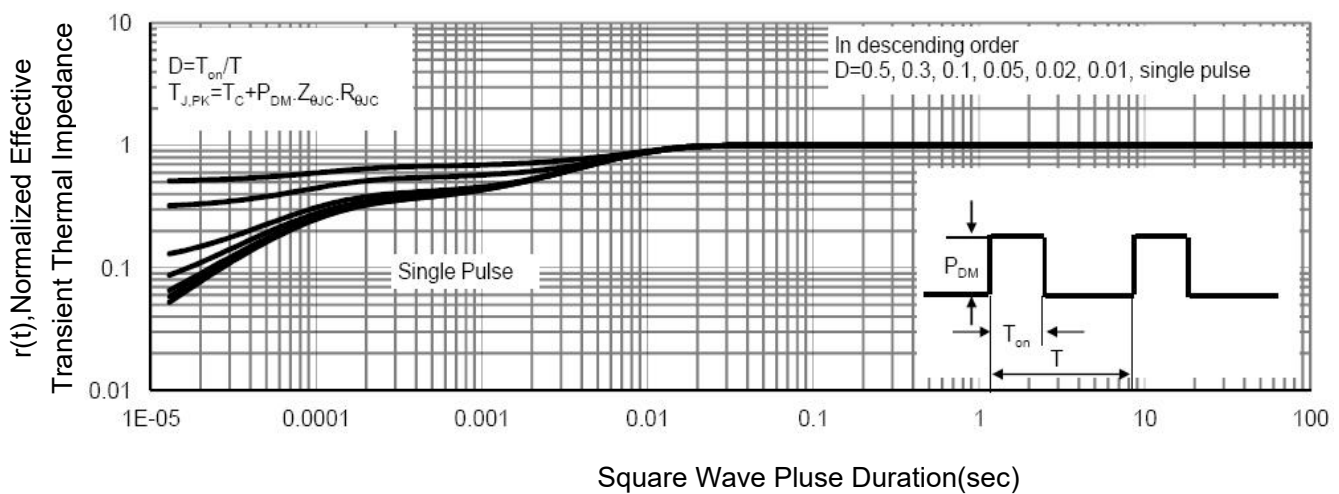
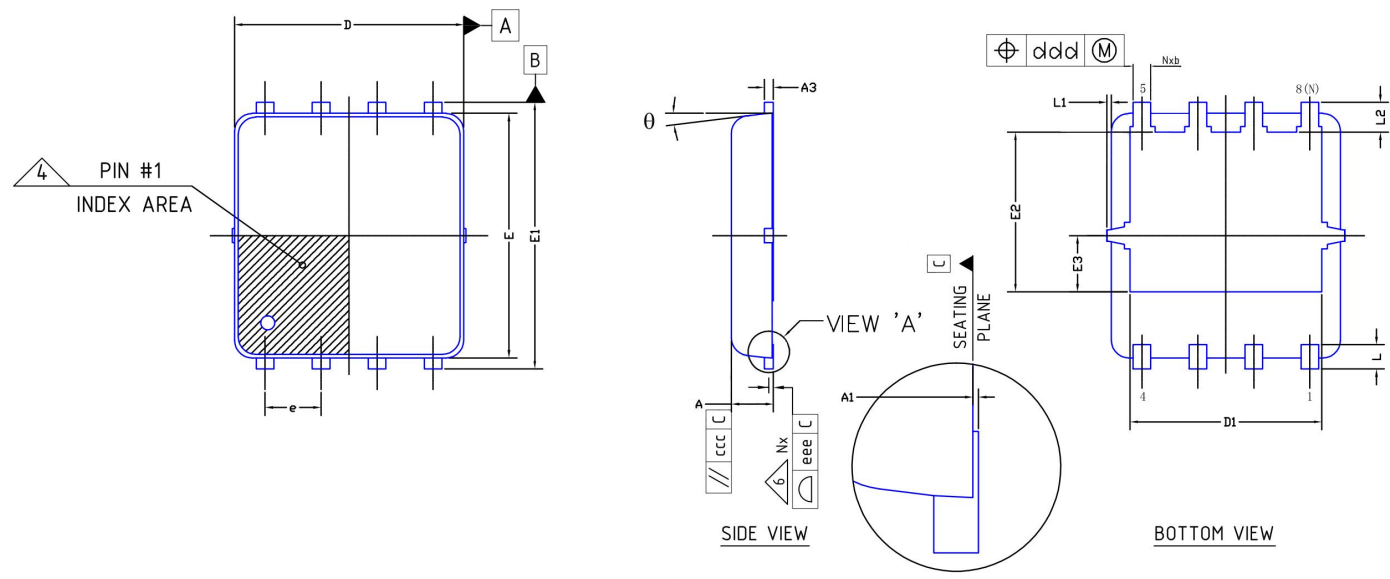


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



Dimension Table				
Thickness Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.85	0.95	1.00	
A1	0.00	---	0.05	
A3	---	0.2 Ref	---	
b	0.30	0.40	0.50	
D	5.20 BSC			
E	5.55 BSC			
e	1.27 BSC			
D1	4.25	4.35	4.45	
E1	5.95	6.05	6.15	
E2	3.525	3.625	3.725	
E3	1.175	1.275	1.375	
L	0.45	0.55	0.65	
L1	0	---	0.15	
L2	0.68 REF			
θ	0°	---	10°	
aaa	0.05			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.08			
N	8			3
ND	4			5
NOTES	1,2			
LF PART NO.	445831/445897			

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.

4. The location of the marked terminal #1 identifier is within the hatched area.

5. NE refers to the maximum number of terminals E side.

6. Coplanarity applies to the terminals and all other bottom surface metallization.

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