

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP018N60GU uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

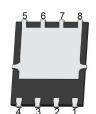
General Features

- V_{DS} =60V,I_D =195A
 - $R_{DS(ON)} {=} 1.5~m\Omega$ (typical) @ $V_{GS} {=} 10 V$
- Excellent gate charge x R_{DS(on)} product(FOM)
- Very low on-resistance R_{DS(on)}
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED! 100% ΔVds TESTED!

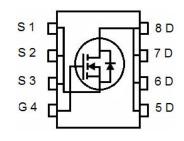
DFN 5X6-8L





Top View

Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P018N60GU	NCEP018N60GU	DFN5X6-8L	-	-	-

Absolute Maximum Ratings (T_c=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V
Gate-Source Voltage	V _G s	±20	V
Drain Current-Continuous	I _D	195	Α
Drain Current-Continuous(T _C =100 °C)	I _D (100℃)	135	А
Pulsed Drain Current	I _{DM}	780	А
Maximum Power Dissipation	P _D	220	W
Derating factor		1.76	W/℃
Single pulse avalanche energy (Note 1)	Eas	871	mJ
Operating Junction and Storage Temperature Range	T_{J}, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case	R _{eJC}	0.57	°C/W
Thermal Resistance,Junction-to-Ambient (Note 4)	R _{0JA}	50	°C/W

NCEP018N60GU

Electrical Characteristics (T_C=25°Cunless otherwise noted)

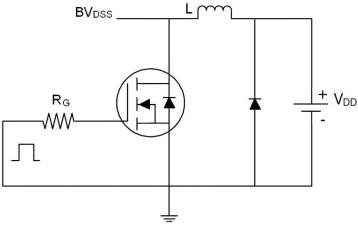
Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS},I_{D}=250\mu A$	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	1.5	1.8	mΩ
Forward Transconductance	g FS	V _{DS} =5V,I _D =20A	-	50	-	S
Dynamic Characteristics						
Input Capacitance	C _{lss}	\/ 00\/\/ 0\/	-	5200	-	PF
Output Capacitance	C _{oss}	V_{DS} =30V, V_{GS} =0V, F=1.0MHz	-	960	-	PF
Reverse Transfer Capacitance	Crss	F=1.UMHZ	-	65	-	PF
Switching Characteristics (Note 2)	·					
Turn-on Delay Time	t _{d(on)}		-	17	-	nS
Turn-on Rise Time	tr	V_{DD} =30 V , I_D =20 A	-	10	-	nS
Turn-Off Delay Time	t _{d(off)}	$V_{GS}\text{=}10V, R_{G}\text{=}4.7\Omega$	-	60	-	nS
Turn-Off Fall Time	t _f		-	18	-	nS
Total Gate Charge	Qg	\/ 00\/ L 00A	-	79		nC
Gate-Source Charge	Q _{gs}	V _{DS} =30V,I _D =20A,	-	25.5		nC
Gate-Drain Charge	Q_{gd}	V _{GS} =10V	-	16		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V,I _S =20A	-		1.2	V
Diode Forward Current	Is		-	-	195	Α
Reverse Recovery Time	t _{rr}	$T_J = 25^{\circ}C$, $I_F = I_S$	-	60		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/μs	-	85		nC

Notes:

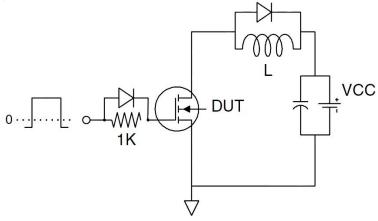
- 1. EAS condition : Tj=25 $^{\circ}\text{C}$,V_DD=30V,V_G=10V,L=0.5mH,Rg=25 Ω
- 2. Guaranteed by design, not subject to production
- 3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=150°C. The SOA curve provides a single pulse rating.
- 4.The value of $R_{\theta JA}$ is measured with the device mounted on $1in^2$ FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

Test Circuit

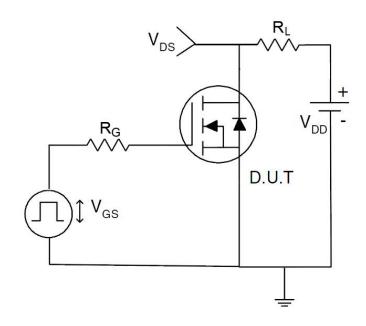
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

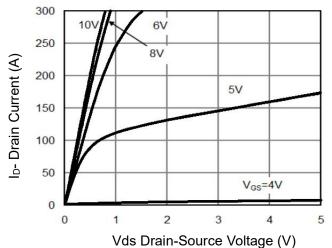


Figure 1 Output Characteristics

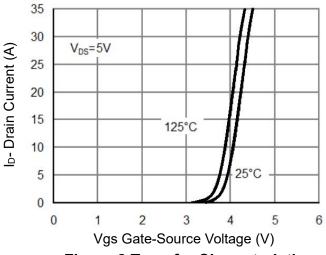


Figure 2 Transfer Characteristics

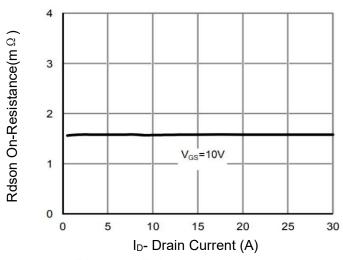


Figure 3 Rdson- Drain Current

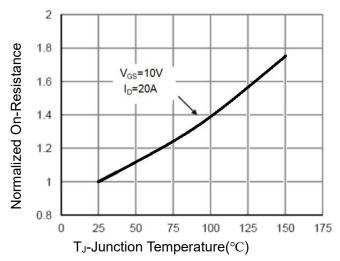


Figure 4 Rdson-JunctionTemperature

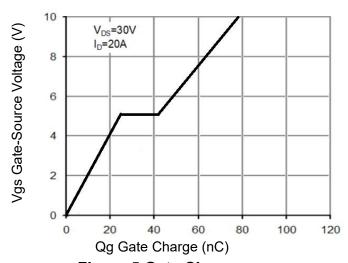


Figure 5 Gate Charge

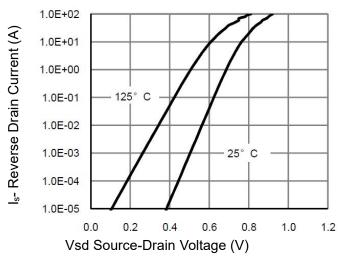
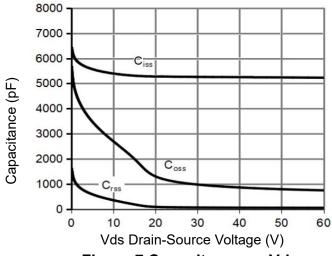


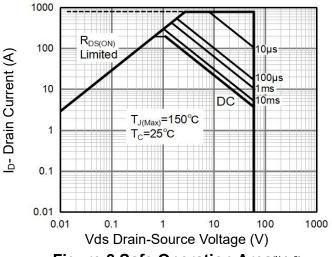
Figure 6 Source- Drain Diode Forward



250

Figure 7 Capacitance vs Vds

Figure 9 Power De-rating



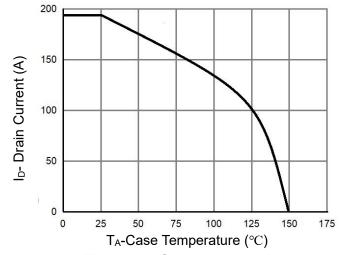


Figure 8 Safe Operation Area(Note 3)

Figure 10 Current De-rating

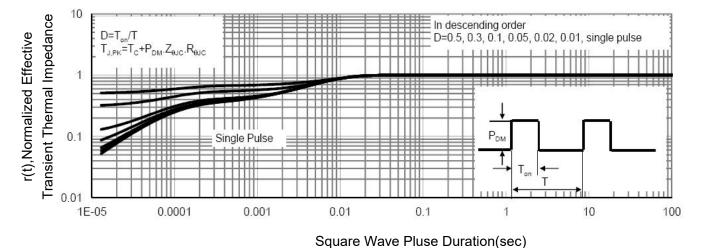
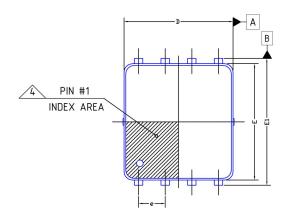
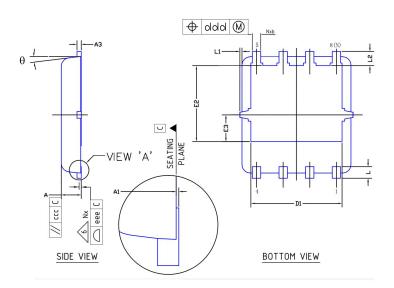


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information





	Dimension Table					
Thickness Symbol	٧			NOTE		
"Mbol "S	MINIMUM	NOMINAL	MAXIMUM			
Α	0.85	0.95	1.00			
A1	0.00		0.05			
A3		0.2 Ref				
ь	0.30	0.40	0.50			
D		5.20 BSC				
E		5.55 BSC				
е		1.27 BSC				
D1	4.25	4.35	4.45			
E1	5.95	6.05	6.15			
E2	3.525	3.625	3.725			
E3	1.175	1.275	1.375			
L	0.45	0.55	0.65			
L1	0		0.15			
L2	0.68 REF					
θ	0° 10°					
aaa	0.05					
bbb	0.10					
CCC	0.10					
ddd	0.05					
eee	0.08					
N	8			3		
ND	4			5		
NOTES	1,2					
LF PART NO.	44					

NOTE:

- 1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
- 2. All dimensions are in millimeters.
- 3. N is the total number of terminals.
- 4. The location of the marked terminal #1 identifier is within the hatched area.
- 5. NE refers to the maximum number of terminals E side.
- 6. Coplanarity applies to the terminals and all other bottom surface metallization.

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