

NCE N-Channel Super Trench Power MOSFET

Description

The NCEP01T13LL uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

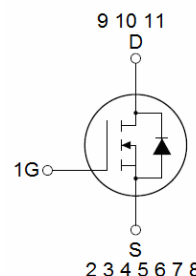
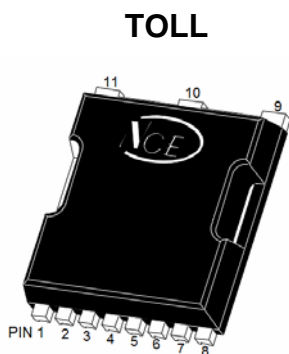
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

- $V_{DS} = 100V, I_D = 160A$
 $R_{DS(ON)} = 3.3m\Omega$, typical@ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!

100% ΔV_{ds} TESTED!



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP01T13LL	NCEP01T13LL	TOLL	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	160	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	128	A
Pulsed Drain Current	I_{DM}	640	A
Maximum Power Dissipation	P_D	260	W
Derating factor		1.73	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	1200	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.58	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

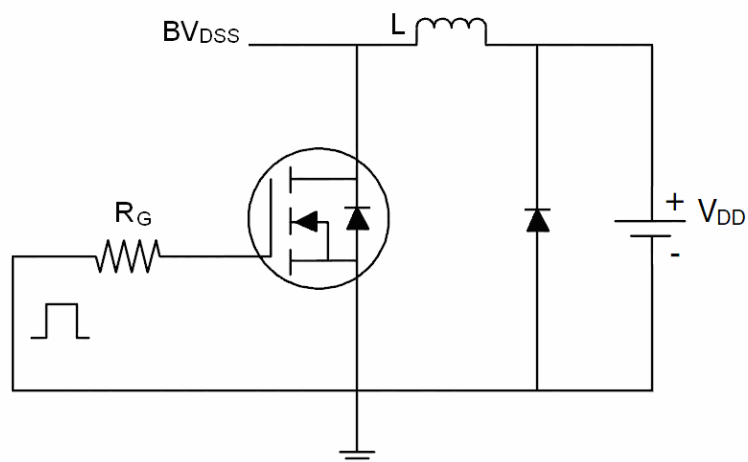
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.3	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =80A	-	3.3	3.9	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =80A	70	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	7500	-	PF
Output Capacitance	C _{oss}		-	755	-	PF
Reverse Transfer Capacitance	C _{rss}		-	45	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =80A V _{GS} =10V, R _G =4.7Ω	-	20	-	nS
Turn-on Rise Time	t _r		-	78	-	nS
Turn-Off Delay Time	t _{d(off)}		-	50	-	nS
Turn-Off Fall Time	t _f		-	16	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =80A, V _{GS} =10V	-	100		nC
Gate-Source Charge	Q _{gs}		-	43.4		nC
Gate-Drain Charge	Q _{gd}		-	19.7		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =160A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	160	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note3)	-	65		nS
Reverse Recovery Charge	Q _{rr}		-	144		nC

Notes:

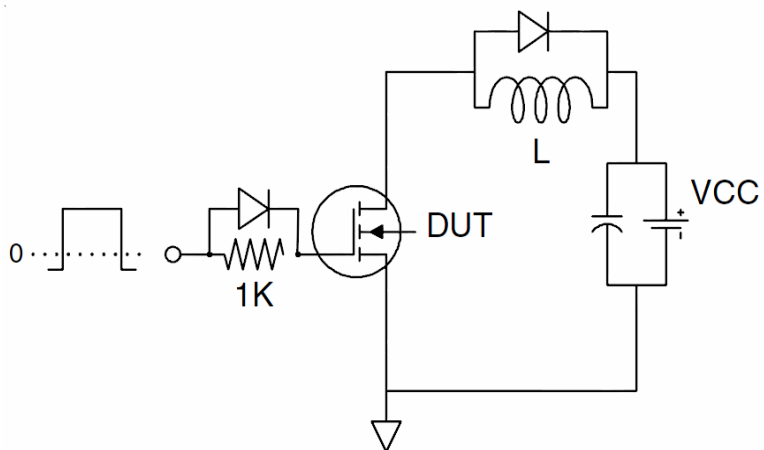
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board by JEDEC . Continuous current at $T_C=25^{\circ}\text{C}$ is silicon limited
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Test Circuit

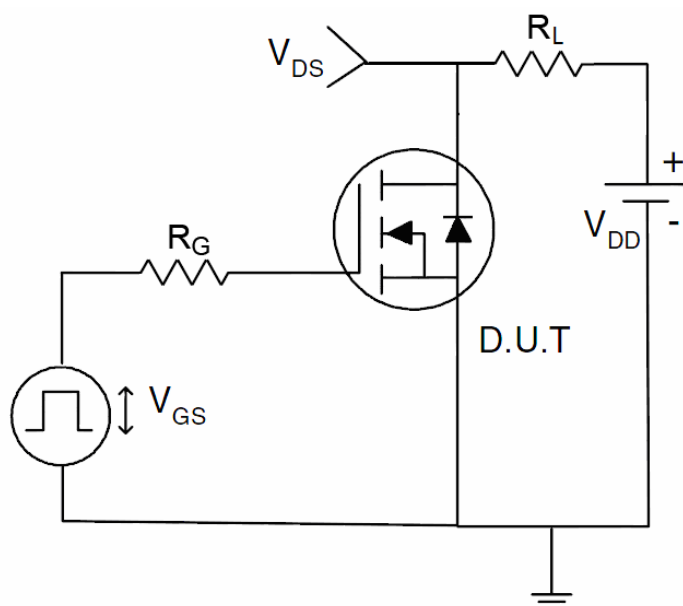
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

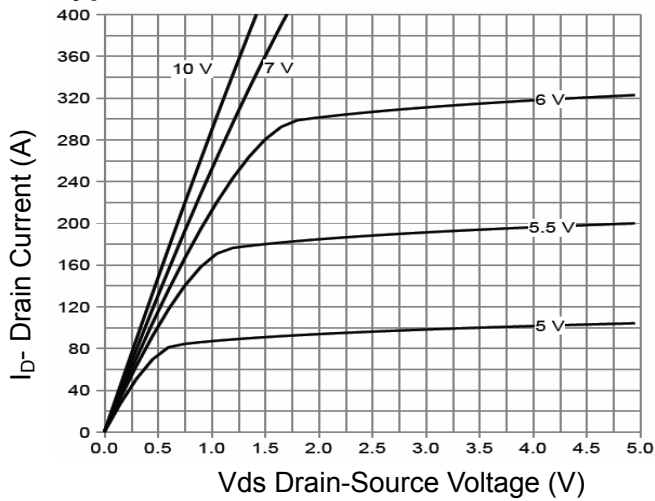


Figure 1 Output Characteristics

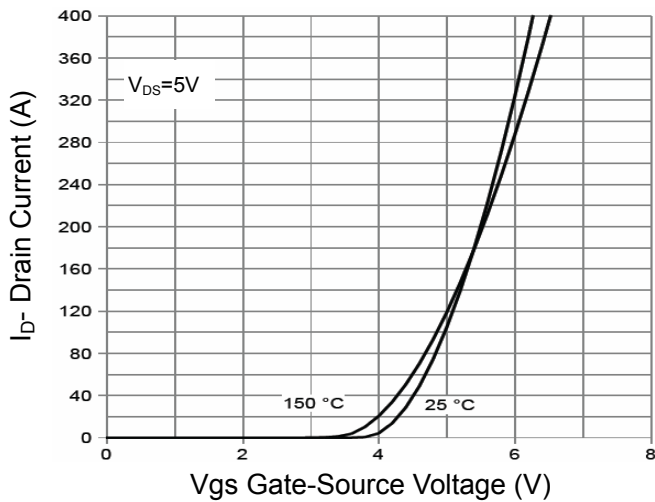


Figure 2 Transfer Characteristics

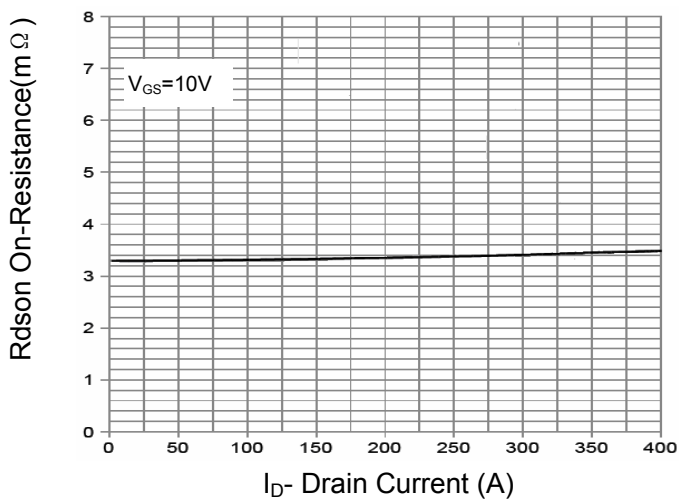


Figure 3 $R_{DS(on)}$ - Drain Current

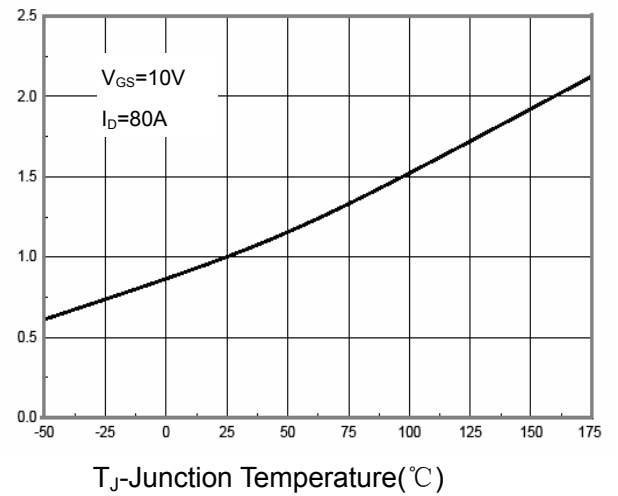


Figure 4 $R_{DS(on)}$ -Junction Temperature

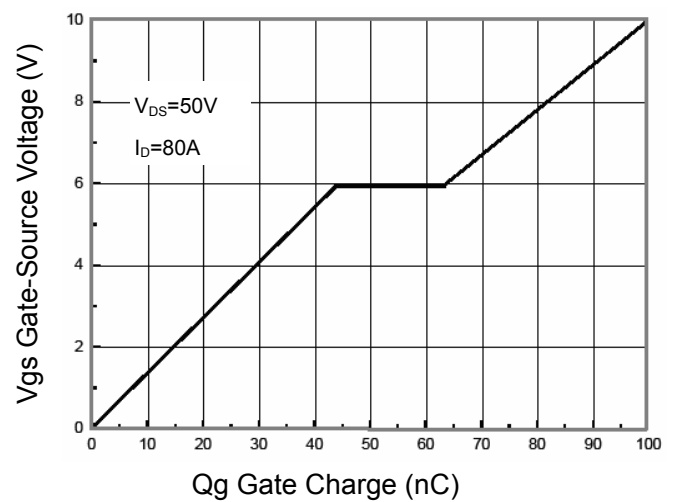


Figure 5 Gate Charge

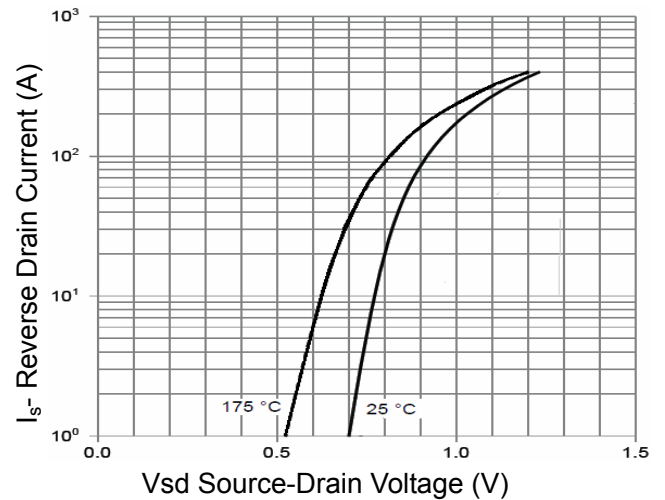


Figure 6 Source- Drain Diode Forward

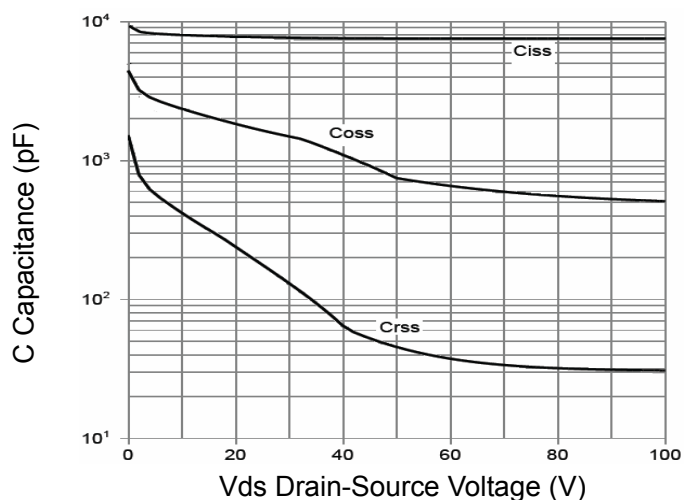


Figure 7 Capacitance vs Vds

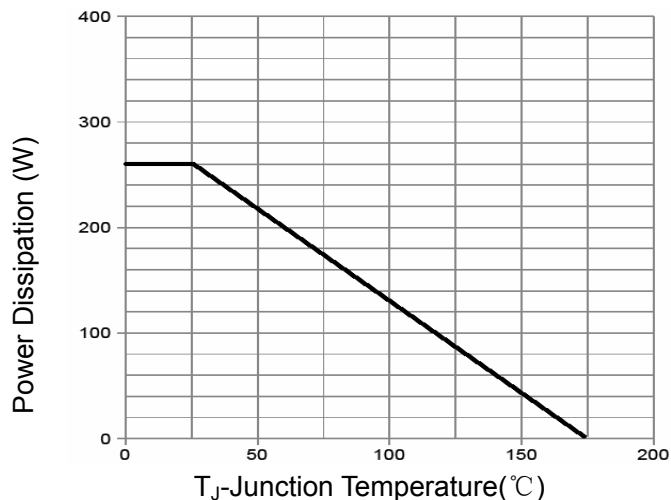


Figure 9 Power De-rating

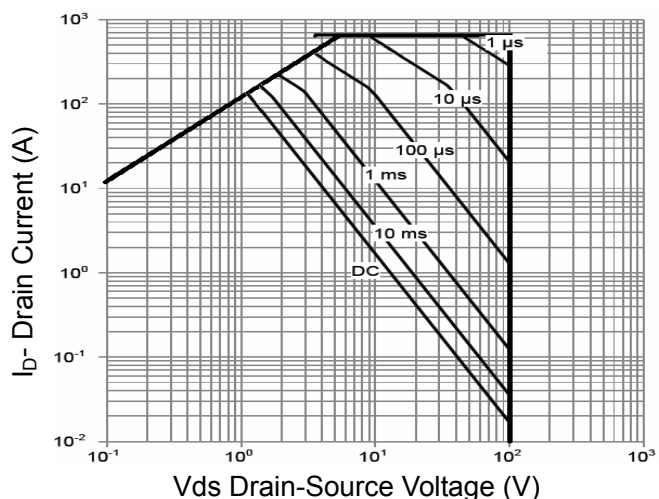


Figure 8 Safe Operation Area

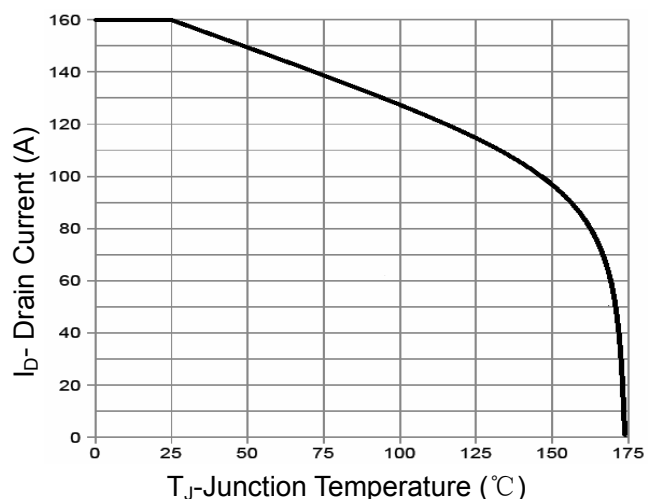


Figure 10 Current De-rating

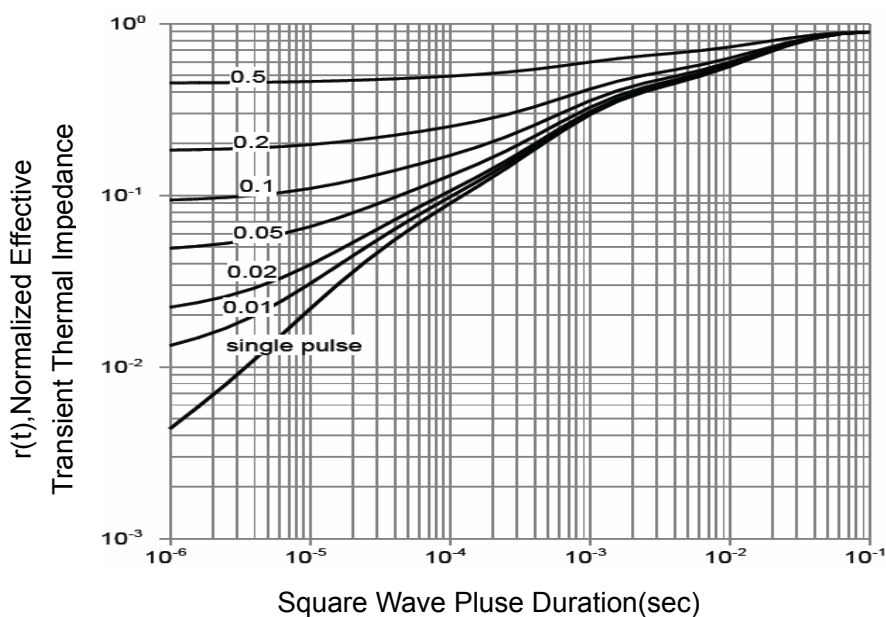
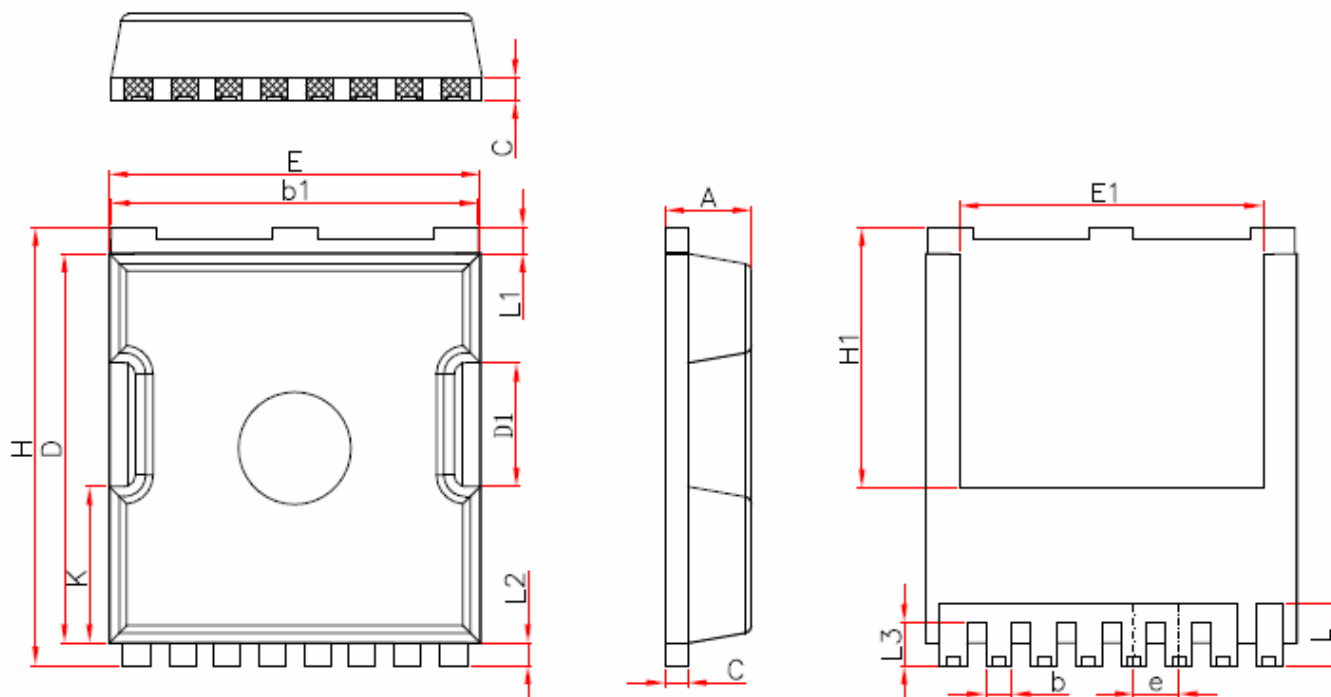


Figure 11 Normalized Maximum Transient Thermal Impedance

TOLL Package Information



Symbol	Millimeters		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
b	0.65	0.75	0.85
b1	9.70	9.80	9.90
C	0.50	0.60	0.70
D	10.30	10.40	10.50
D1	3.15	3.3	3.45
E	9.70	9.90	10.10
E1	8.00	8.10	8.20
e	1.10	1.20	1.30
H	11.6	11.7	11.8
H1	6.85	6.95	7.05
K	4.08	4.18	4.28
L	1.60	1.65	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	1.05	1.20	1.30

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