

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP025N60AG uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

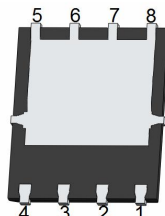
- $V_{DS} = 60V, I_D = 165A$
 $R_{DS(ON)} = 2.0m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 2.5m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

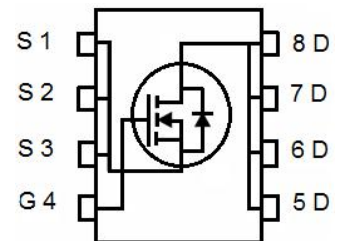
DFN 5X6



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P025N60AG	NCEP025N60AG	DFN5X6-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	165	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	115	A
Pulsed Drain Current	I_{DM}	660	A
Maximum Power Dissipation	P_D	200	W
Derating factor		1.16	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	540	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	0.625	$^\circ C/W$
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Electrical Characteristics (T_c=25°C unless otherwise noted)

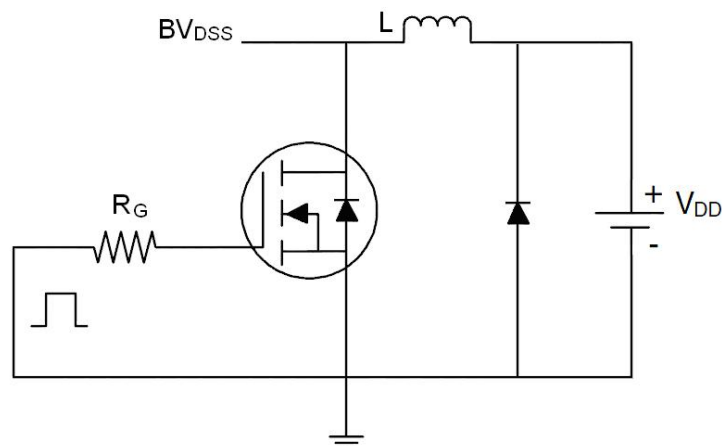
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	60		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics <small>(Note 3)</small>						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	1.7	2.4	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =82.5A	-	2.0	2.5	mΩ
		V _{GS} =4.5V, I _D =82.5A	-	2.5	3.7	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =82.5A	45	-	-	S
Dynamic Characteristics <small>(Note4)</small>						
Input Capacitance	C _{iss}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	6540	-	PF
Output Capacitance	C _{oss}		-	900	-	PF
Reverse Transfer Capacitance	C _{rss}		-	65	-	PF
Switching Characteristics <small>(Note 4)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, I _D =82.5A V _{GS} =10V, R _G =4.7Ω	-	16	-	nS
Turn-on Rise Time	t _r		-	9	-	nS
Turn-Off Delay Time	t _{d(off)}		-	58	-	nS
Turn-Off Fall Time	t _f		-	12	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =82.5A, V _{GS} =10V	-	105		nC
Gate-Source Charge	Q _{gs}		-	17.5		nC
Gate-Drain Charge	Q _{gd}		-	17		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage <small>(Note 3)</small>	V _{SD}	V _{GS} =0V, I _S =82.5A	-		1.2	V
Diode Forward Current <small>(Note 2)</small>	I _S		-	-	165	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = I _S di/dt = 100A/μs ^(Note3)	-	56		nS
Reverse Recovery Charge	Q _{rr}		-	80		nC

Notes:

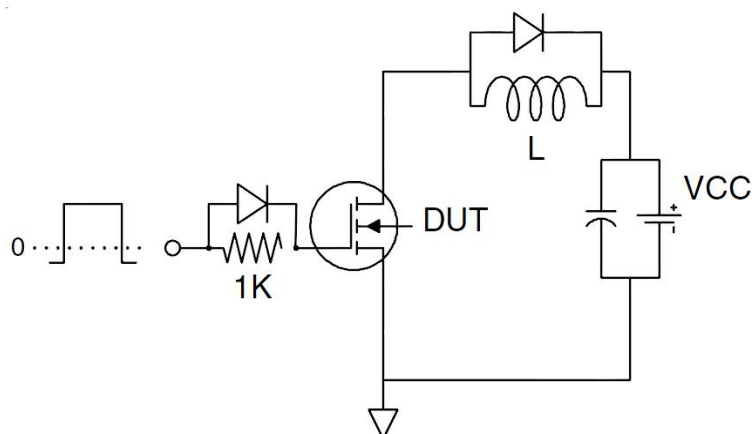
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition : T_J=25°C, V_{DD}=30V, V_G=10V, L=0.5mH, R_G=25Ω

Test Circuit

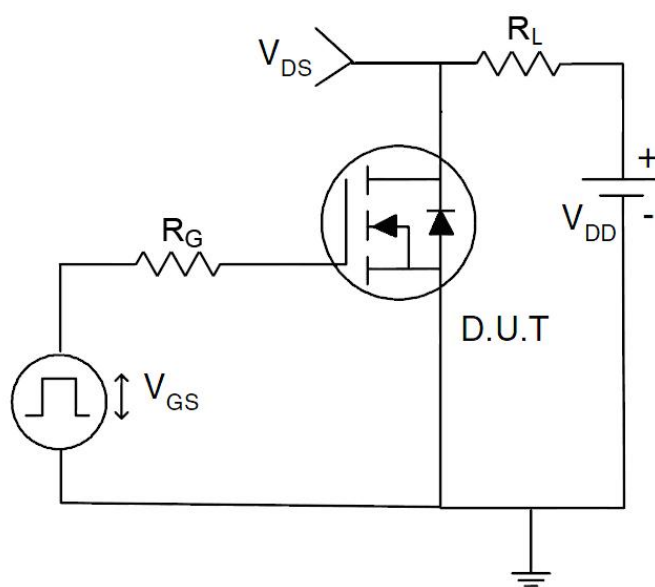
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

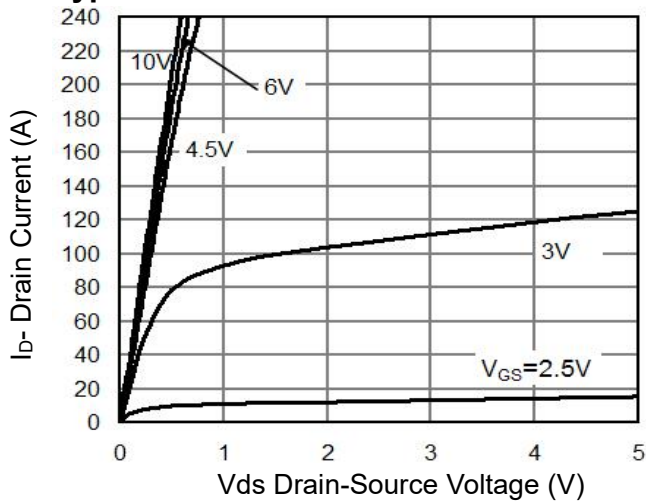


Figure 1 Output Characteristics

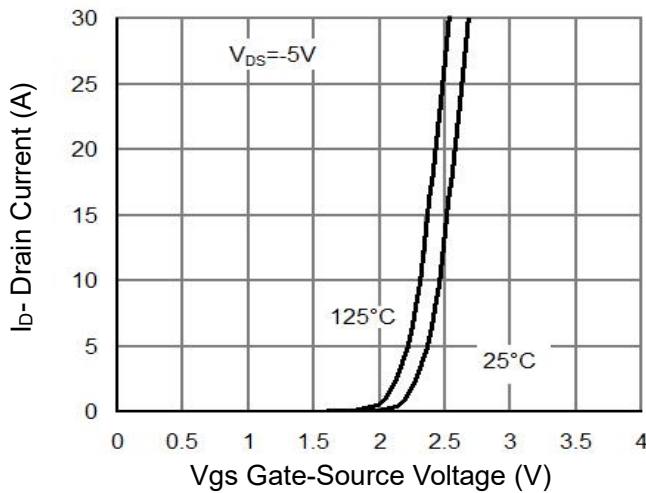


Figure 2 Transfer Characteristics

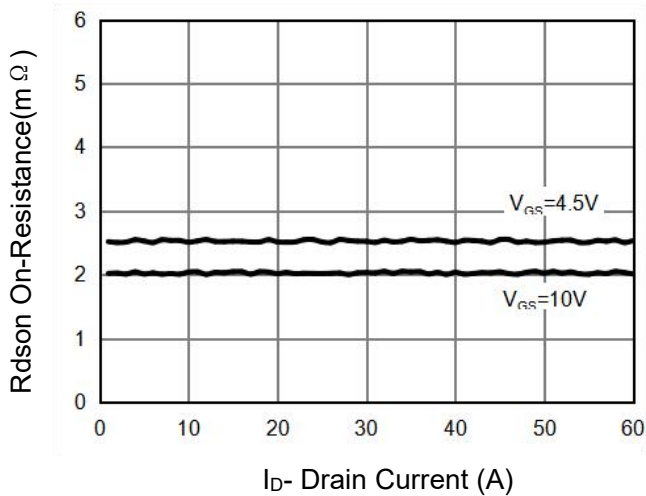


Figure 3 $R_{DS(on)}$ - Drain Current

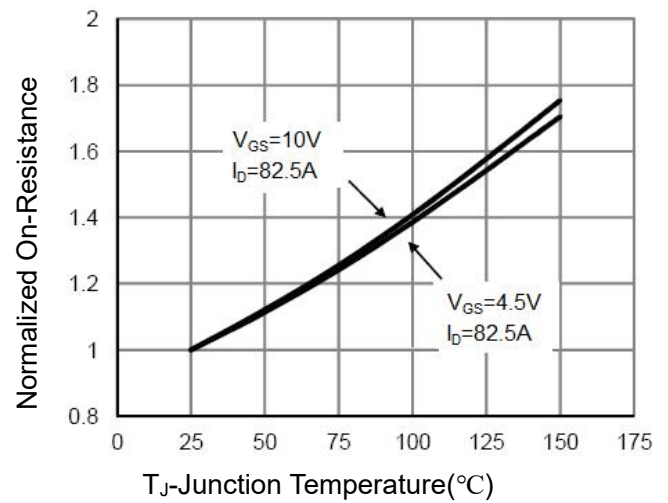


Figure 4 $R_{DS(on)}$ -Junction Temperature

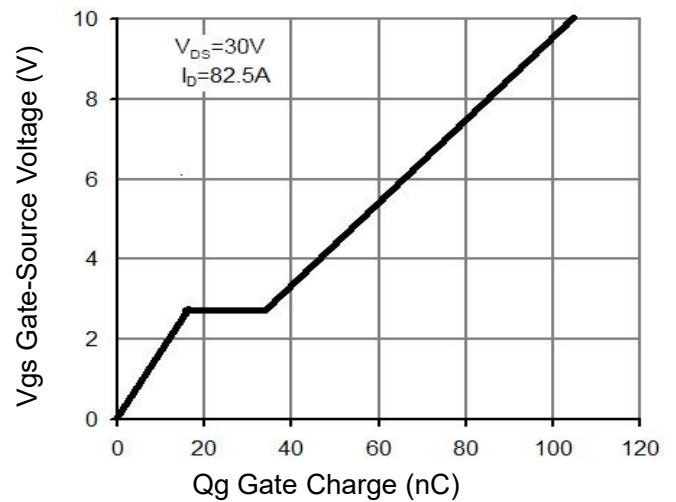


Figure 5 Gate Charge

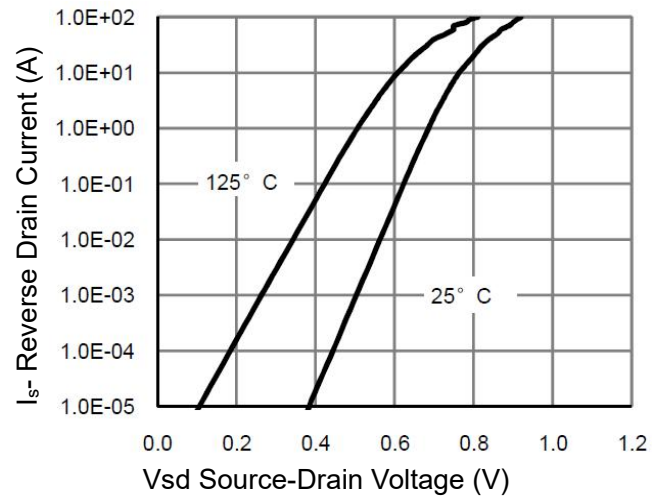


Figure 6 Source- Drain Diode Forward

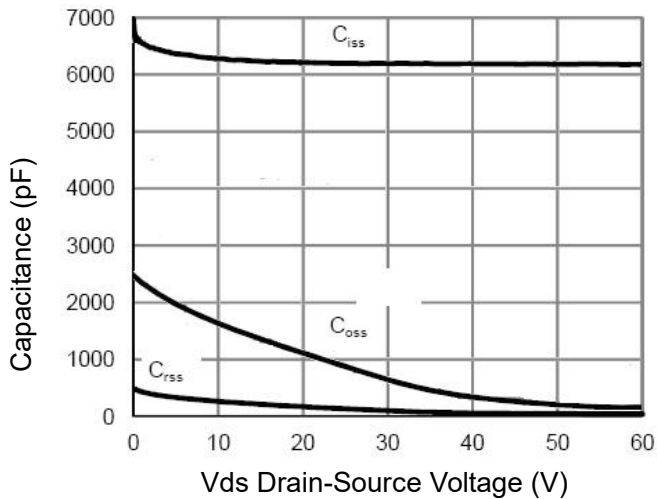


Figure 7 Capacitance vs Vds

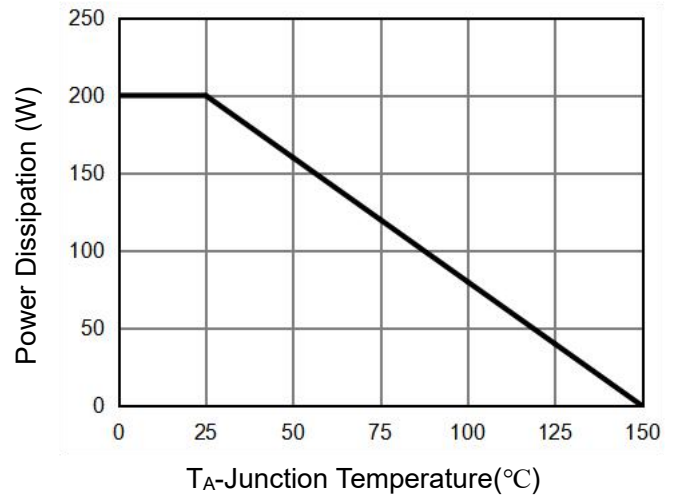


Figure 9 Power De-rating

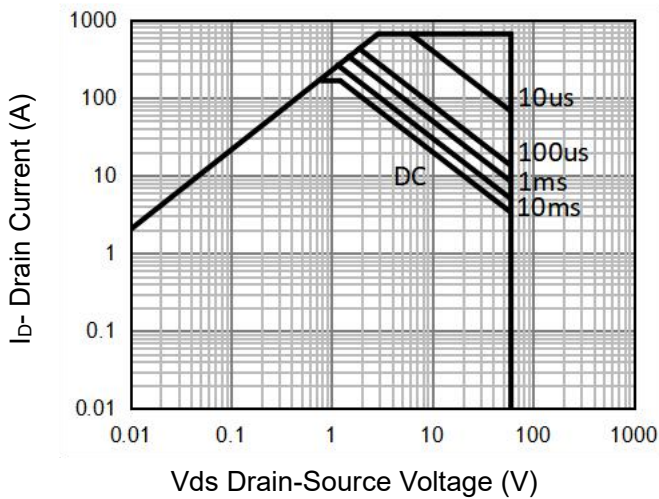


Figure 8 Safe Operation Area

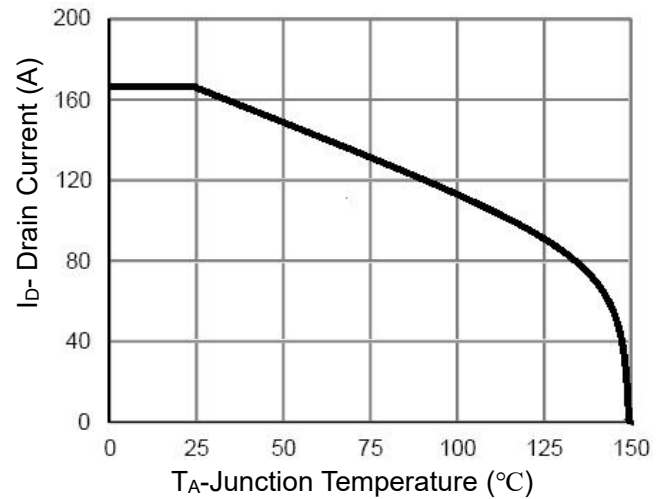


Figure 10 Current De-rating

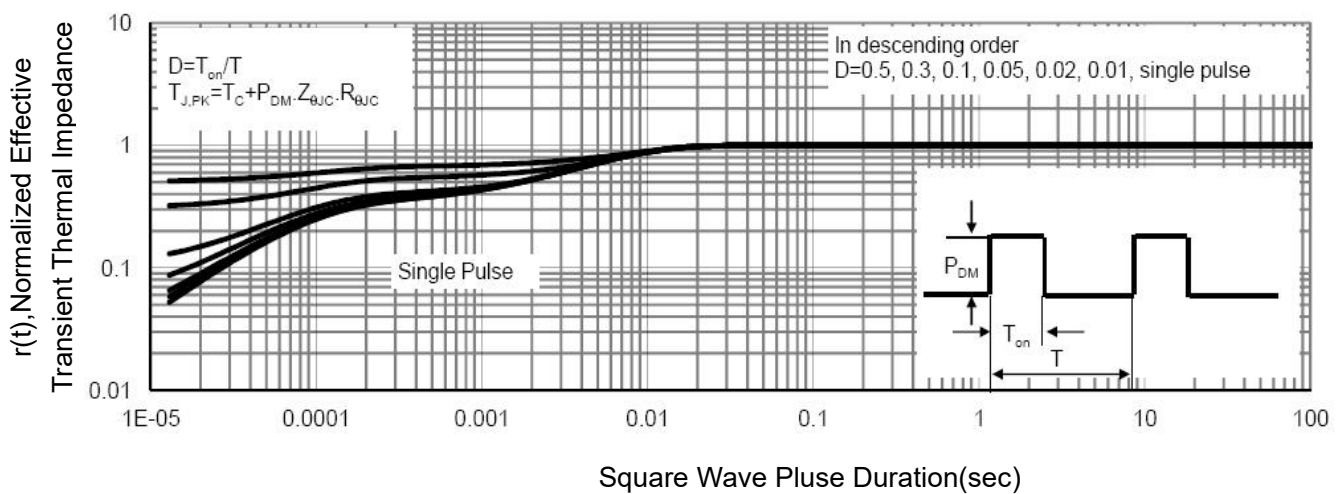
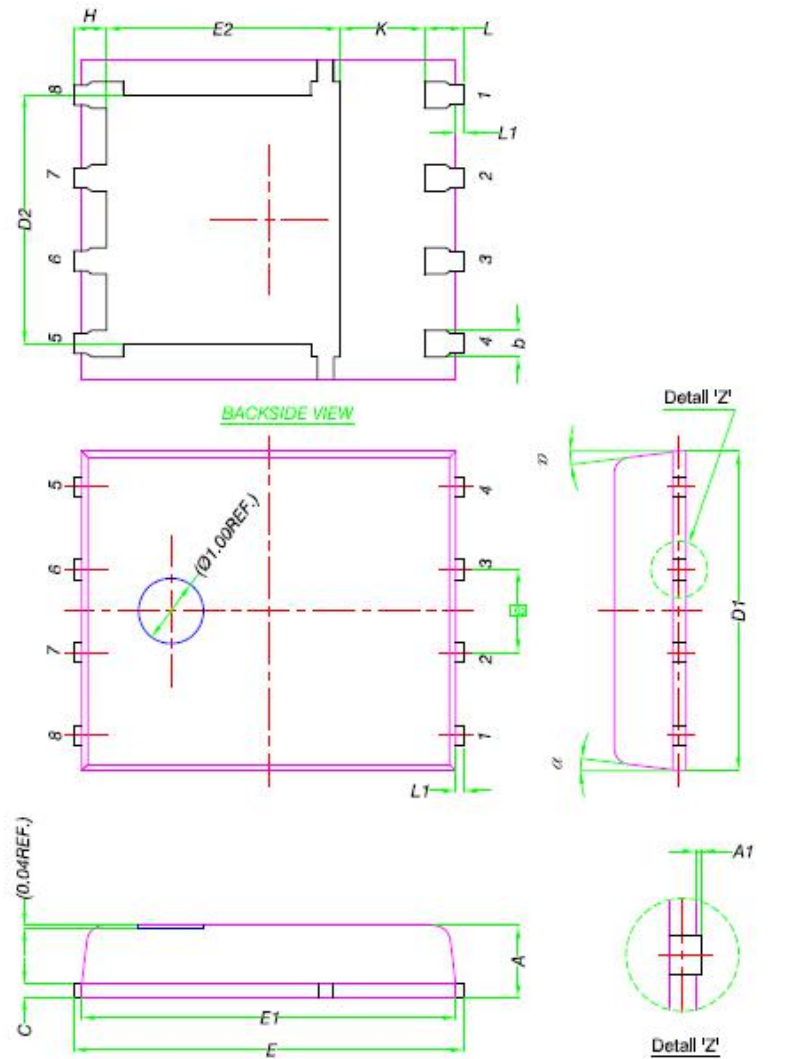

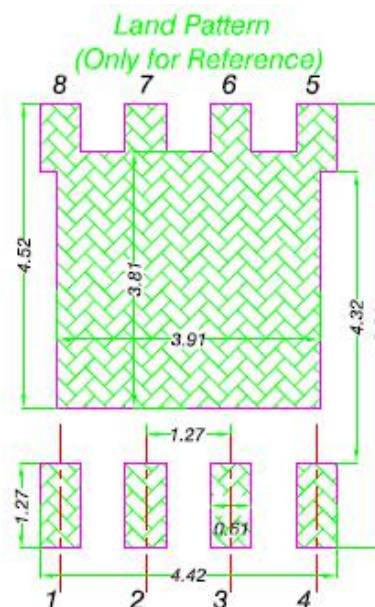


Figure 11 Normalized Maximum Transient Thermal Impedance

DFN5X6-8L Package Information



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°



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