

NCE N-Channel **Super Trench II** Power MOSFET

Description

The series of devices uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

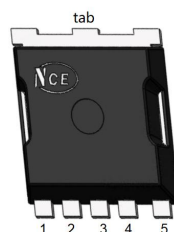
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

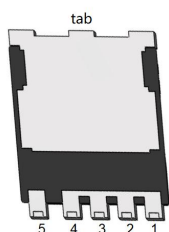
- $V_{DS} = 100V, I_D = 215A$
 $R_{DS(ON)} = 3.0m\Omega$, typical @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- **Pb-free lead plating**
- **Pb-free Mold Compound**

100% UIS TESTED!
100% ΔV_{ds} TESTED!

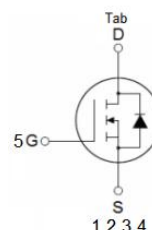
sTOLL



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
P036N10MSL	NCEP036N10MSL	sTOLL	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	215	A
Drain Current-Continuous($T_c = 100^\circ\text{C}$)	$I_D(100^\circ\text{C})$	151	A
Pulsed Drain Current	I_{DM}	860	A
Maximum Power Dissipation	P_D	310	W
Derating factor		2.07	W/ $^\circ\text{C}$
Single pulse avalanche energy ^(Note1)	E_{AS}	1239	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.48	$^\circ\text{C/W}$
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Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.0	3.0	4.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.0	3.55	mΩ
Forward Transconductance	g _{FS}	V _{DS} =15V, I _D =20A		70	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	9500	-	PF
Output Capacitance	C _{oss}		-	650	-	PF
Reverse Transfer Capacitance	C _{rss}		-	40	-	PF
Switching Characteristics <small>(Note 2)</small>						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =20A V _{GS} =10V, R _G =1.6Ω	-	20	-	nS
Turn-on Rise Time	t _r		-	11.5	-	nS
Turn-Off Delay Time	t _{d(off)}		-	48	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =20A, V _{GS} =10V	-	125	-	nC
Gate-Source Charge	Q _{gs}		-	40.5	-	nC
Gate-Drain Charge	Q _{gd}		-	33	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =20A	-		1.2	V
Diode Forward Current	I _S		-	-	215	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 100A di/dt = 100A/μs	-	76	-	nS
Reverse Recovery Charge	Q _{rr}		-	150	-	nC

Notes:

1. EAS condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_J(MAX)=175°C. The SOA curve provides a single pulse rating.

Typical Electrical and Thermal Characteristics

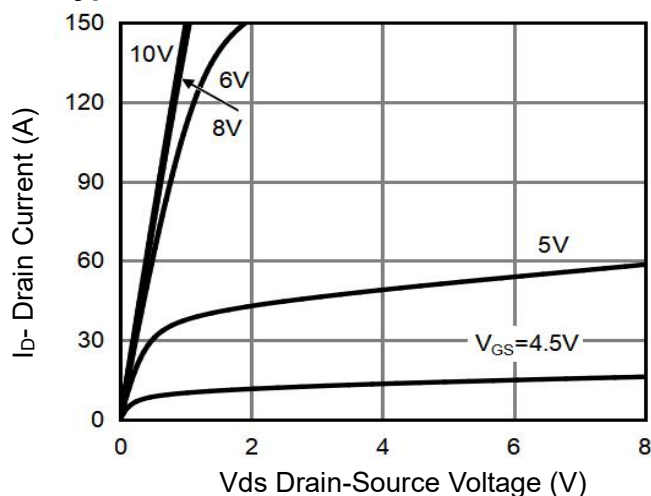


Figure 1 Output Characteristics

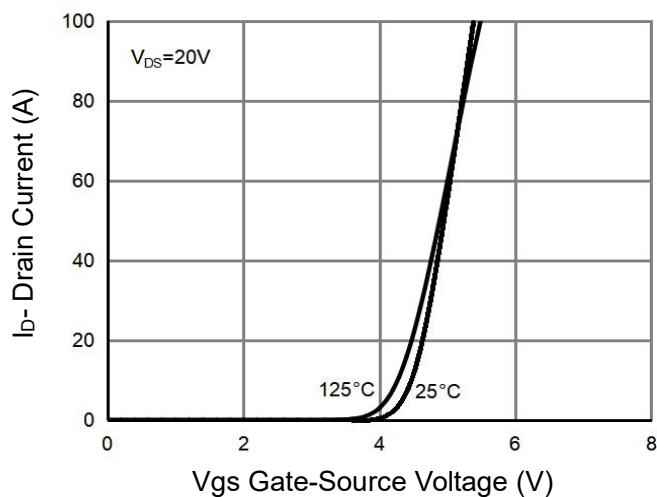


Figure 2 Transfer Characteristics

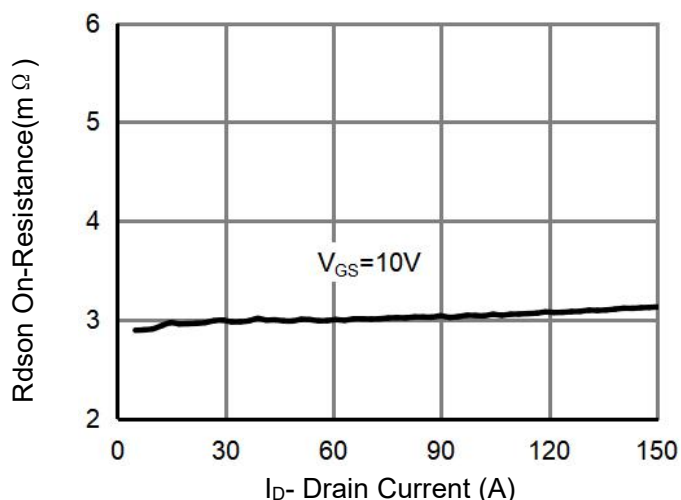


Figure 3 Rdson- Drain Current

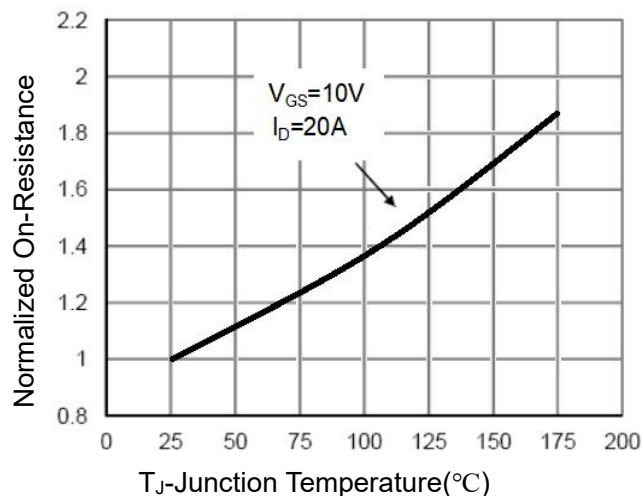


Figure 4 Rdson-Junction Temperature

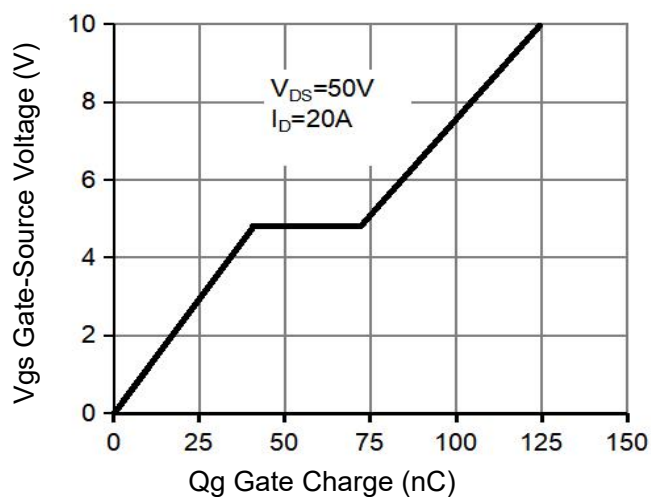


Figure 5 Gate Charge

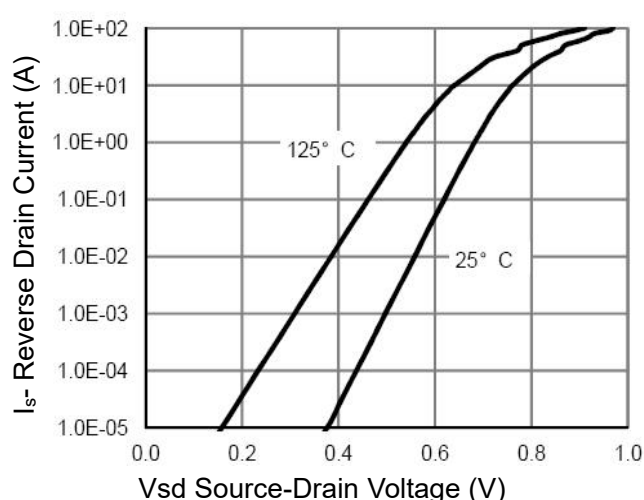


Figure 6 Source- Drain Diode Forward

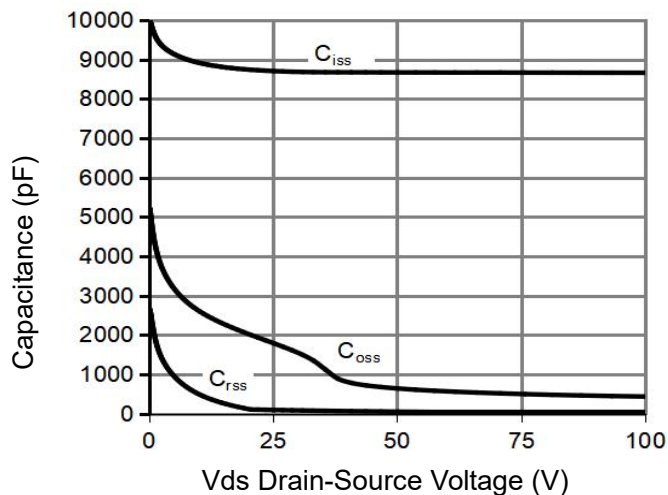


Figure 7 Capacitance vs Vds

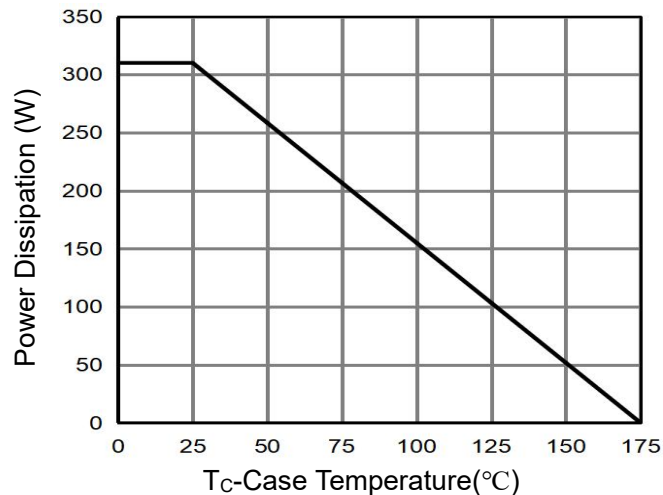


Figure 9 Power De-rating

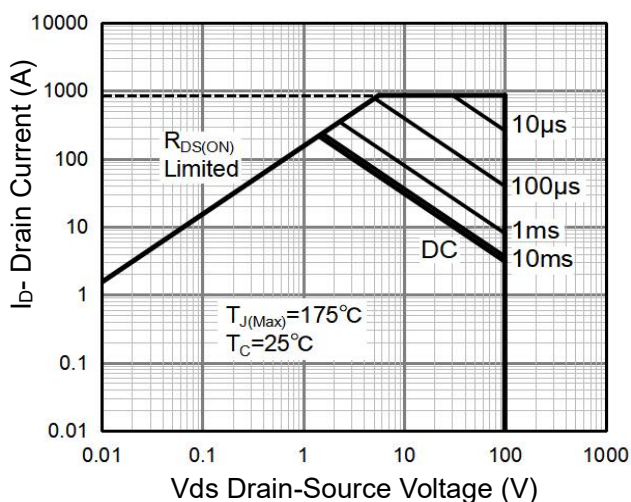


Figure 8 Safe Operation Area (Note3)

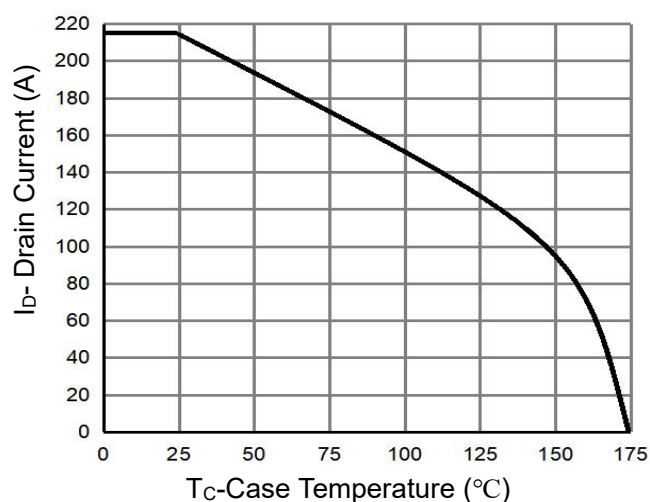


Figure 10 Current De-rating

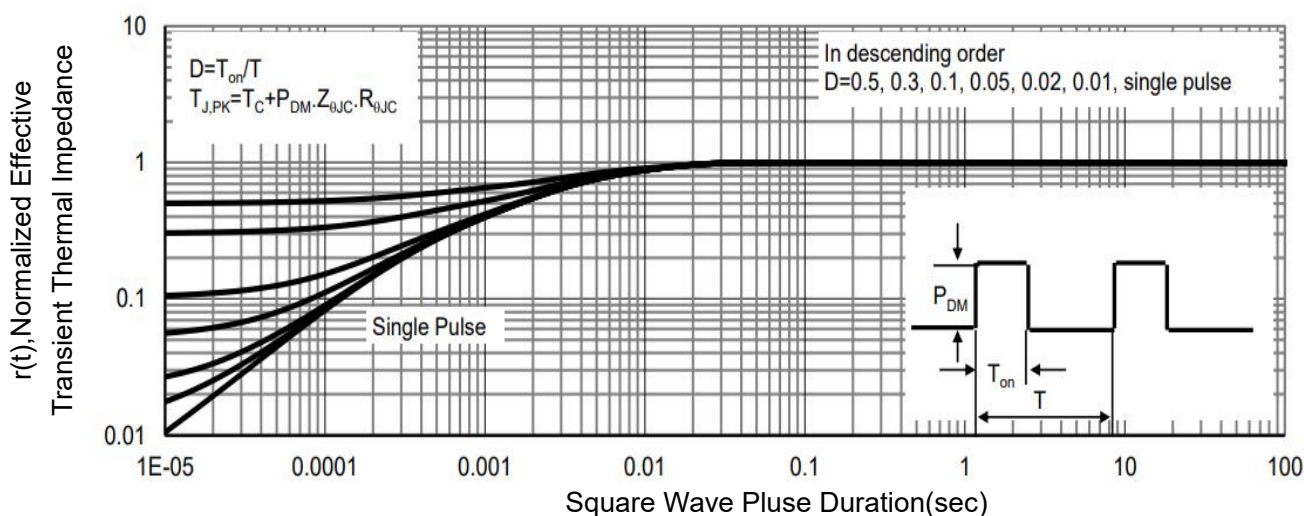
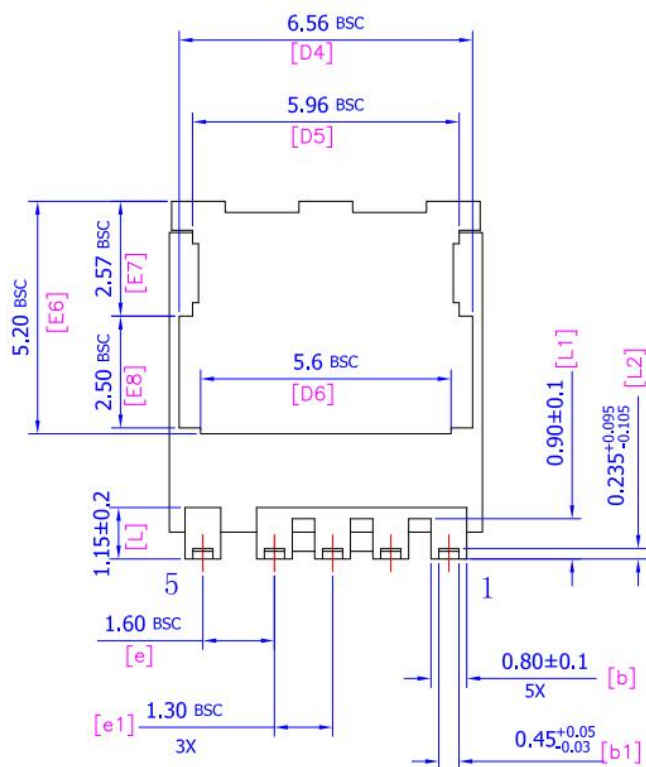
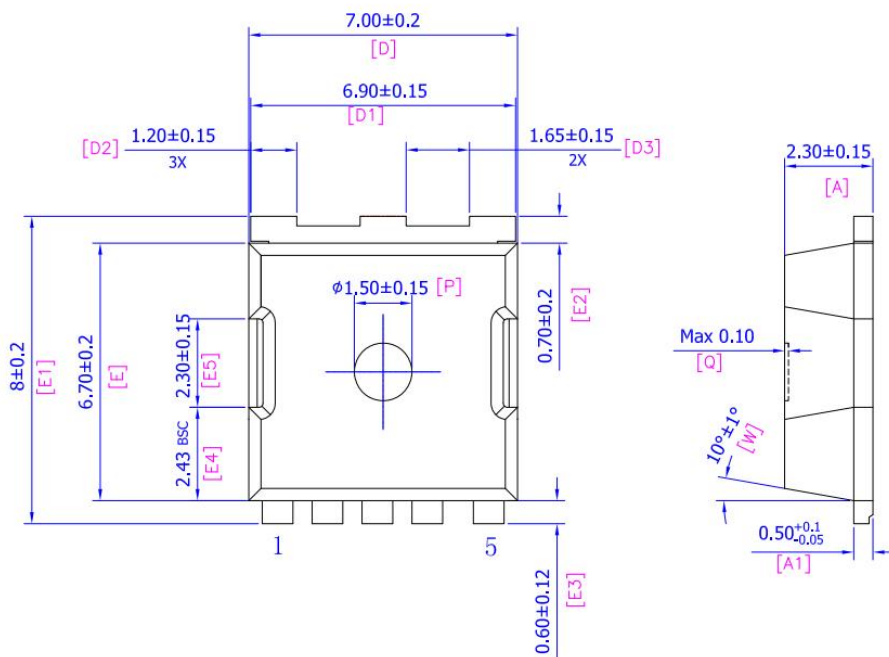


Figure 11 Normalized Maximum Transient Thermal Impedance

sTOLL Package Information



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