

NCE N-Channel Super Trench III Power MOSFET

Description

The series of devices uses **Super Trench III** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

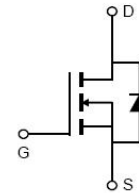
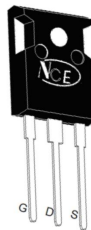
General Features

- $V_{DS} = 150V, I_D = 223A$ (Silicon Limited)
 $R_{DS(ON)} = 3.9m\Omega$, typical @ $V_{GS} = 10V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!

100% ΔV_{ds} TESTED!

TO-247-3L



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP048NH150T	NCEP048NH150T	TO-247-3L	-	-	-

Absolute Maximum Ratings ($T_c = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous (Silicon Limited)	I_D	223	A
Drain Current-Continuous (Package Limited)	I_D	180	A
Drain Current-Continuous($T_c = 100^\circ C$)	$I_D(100^\circ C)$	156	A
Pulsed Drain Current	I_{DM}	720	A
Maximum Power Dissipation	P_D	515	W
Derating factor		3.43	W/ $^\circ C$
Single pulse avalanche energy ^(Note 1)	E_{AS}	1536	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.29	$^\circ C/W$
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Electrical Characteristics (T_C=25°C unless otherwise noted)

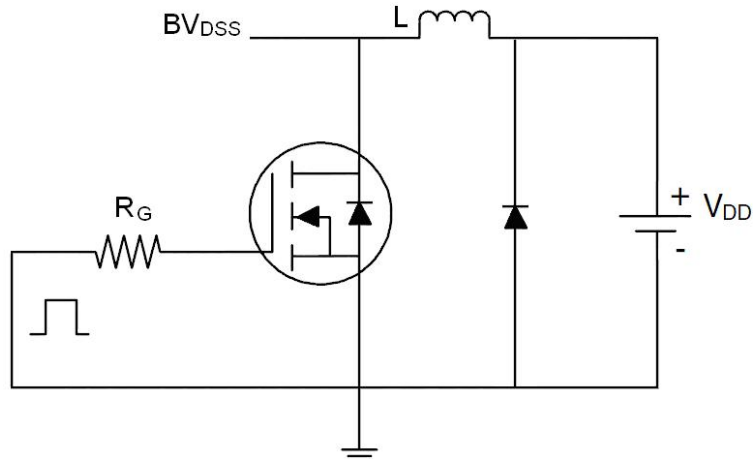
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	150	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	2.5	3.5	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =20A	-	3.9	4.8	mΩ
Forward Transconductance	g _{FS}	V _{DS} =10V, I _D =40A	-	75	-	S
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} =75V, V _{GS} =0V, F=1.0MHz	-	7150	-	PF
Output Capacitance	C _{oss}		-	2050	-	PF
Reverse Transfer Capacitance	C _{rss}		-	47	-	PF
Switching Characteristics (Note 2)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V, I _D =75A V _{GS} =10V, R _G =4.7Ω	-	30	-	nS
Turn-on Rise Time	t _r		-	40	-	nS
Turn-Off Delay Time	t _{d(off)}		-	70	-	nS
Turn-Off Fall Time	t _f		-	15	-	nS
Total Gate Charge	Q _g	V _{DS} =75V, I _D =20A, V _{GS} =10V	-	106	-	nC
Gate-Source Charge	Q _{gs}		-	36	-	nC
Gate-Drain Charge	Q _{gd}		-	27	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _F = I _S	-	-	1.2	V
Diode Forward Current	I _S		-	-	180	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 100A di/dt = 100A/μs	-	108	-	nS
Reverse Recovery Charge	Q _{rr}		-	270	-	nC

Notes:

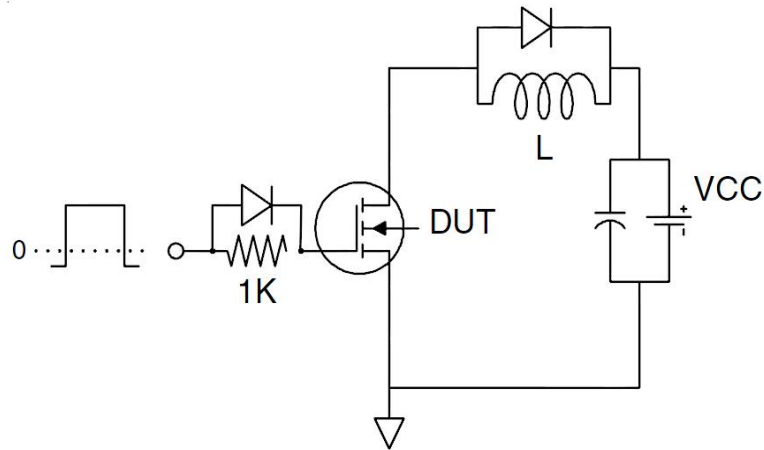
1. EAS condition : T_J=25°C, V_{DD}=50V, V_G=10V, L=0.5mH, R_G=25Ω
2. Guaranteed by design, not subject to production
3. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

Test Circuit

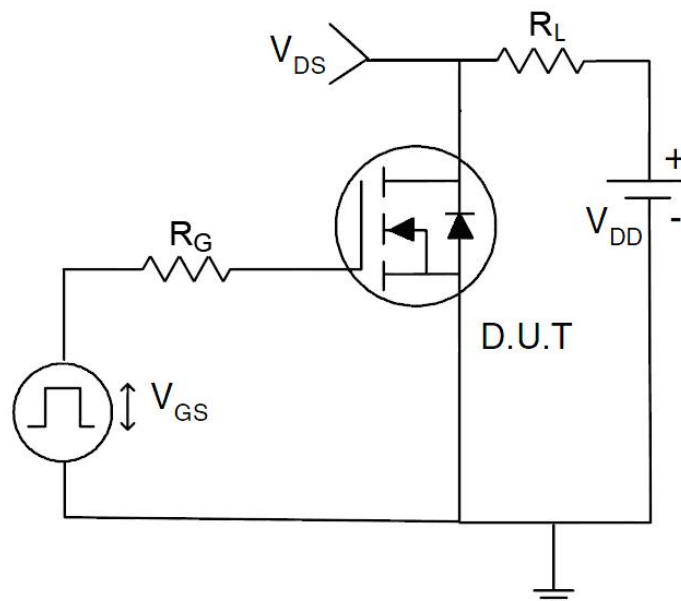
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



Typical Electrical and Thermal Characteristics

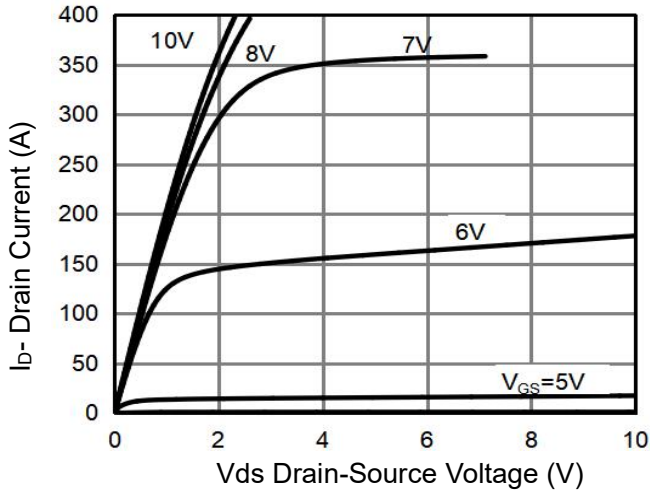


Figure 1 Output Characteristics

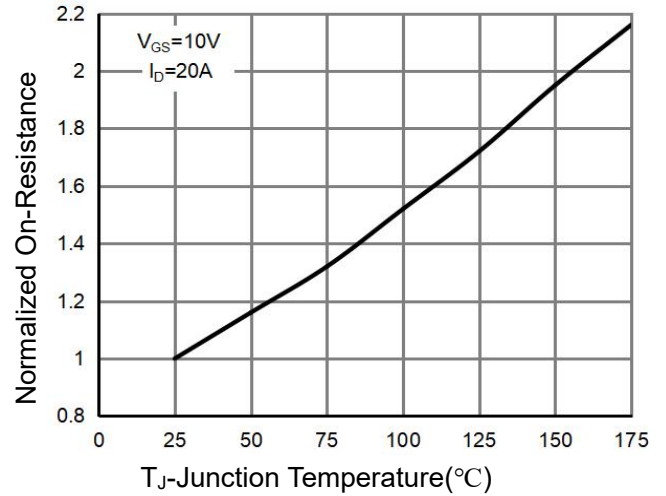


Figure 4 $R_{ds(on)}$ -Junction Temperature

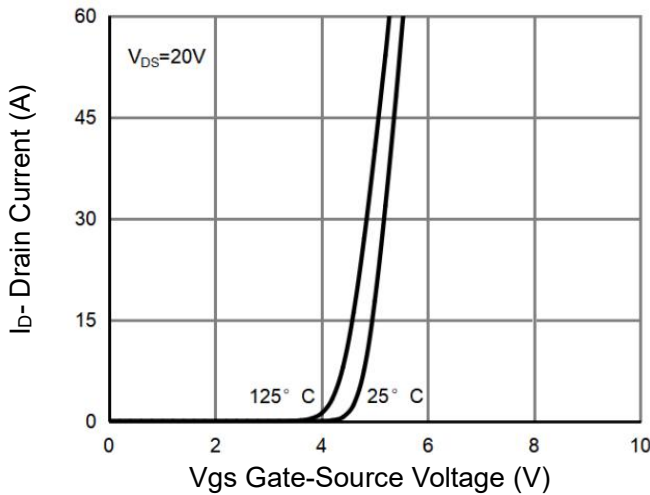


Figure 2 Transfer Characteristics

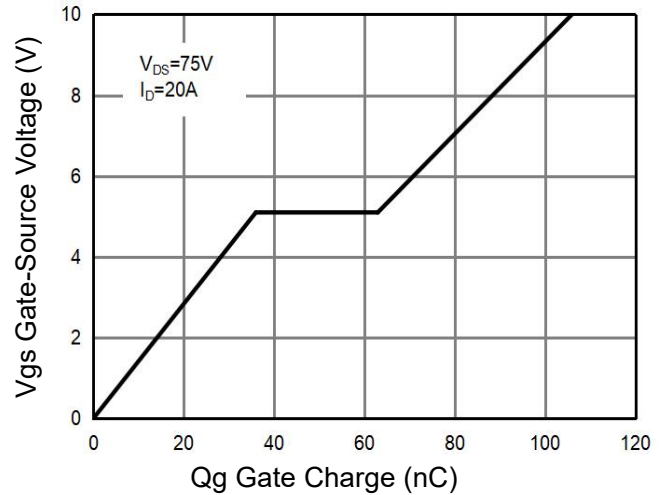


Figure 5 Gate Charge

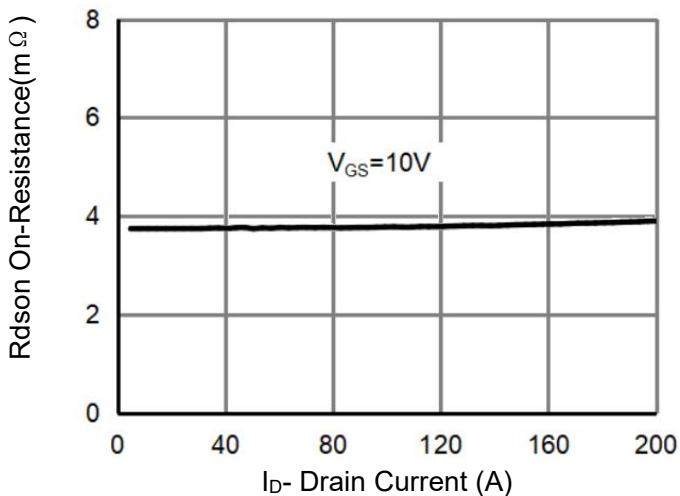


Figure 3 $R_{ds(on)}$ - Drain Current

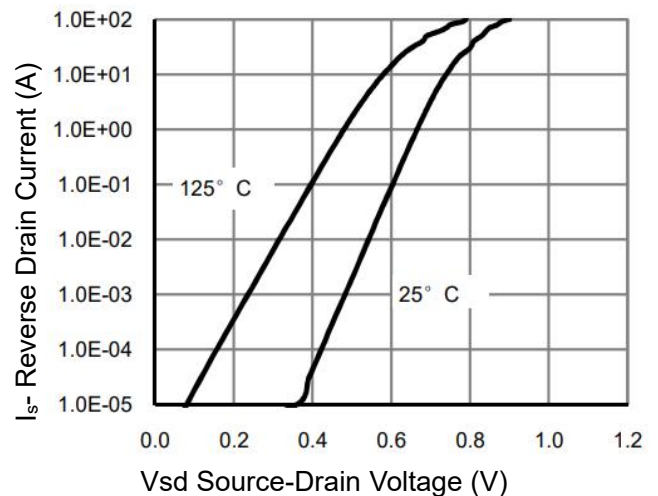


Figure 6 Source- Drain Diode Forward

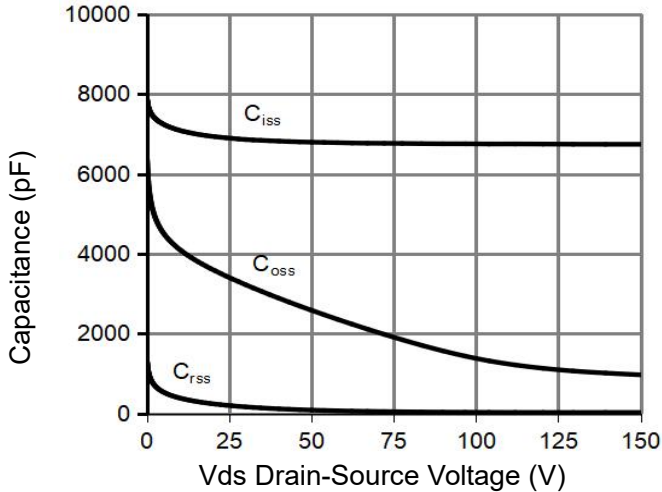


Figure 7 Capacitance vs Vds

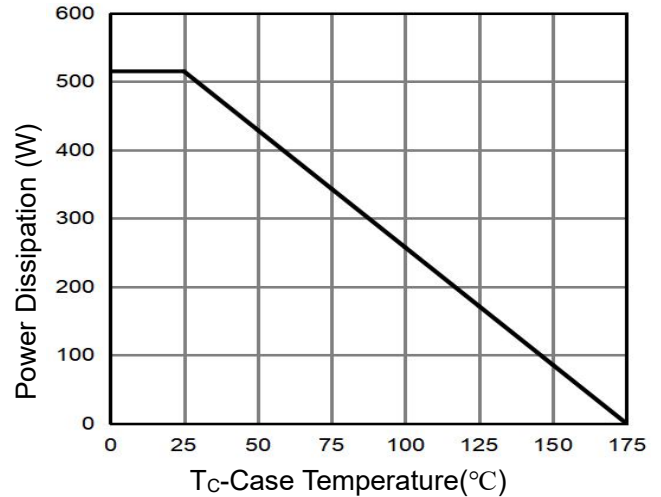


Figure 10 Power De-rating

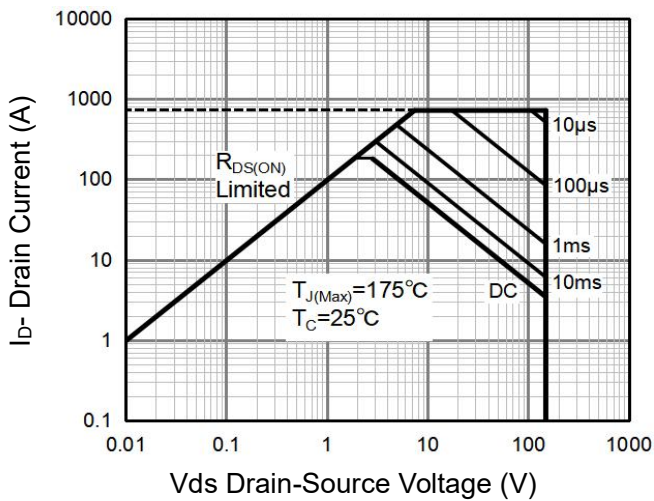


Figure 8 Safe Operation Area (Note3)

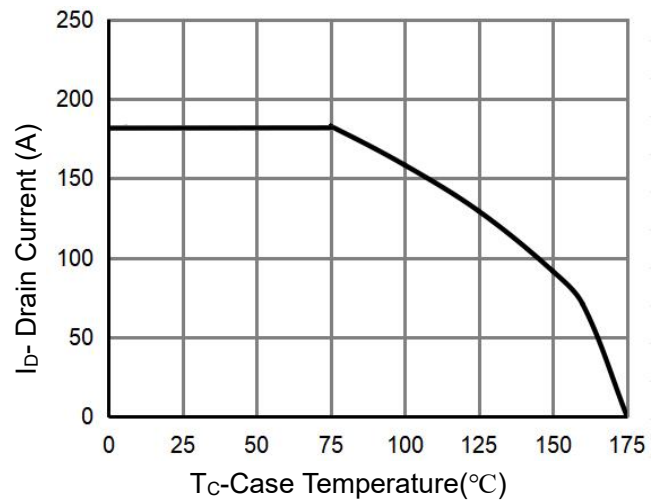


Figure 11 Current De-rating

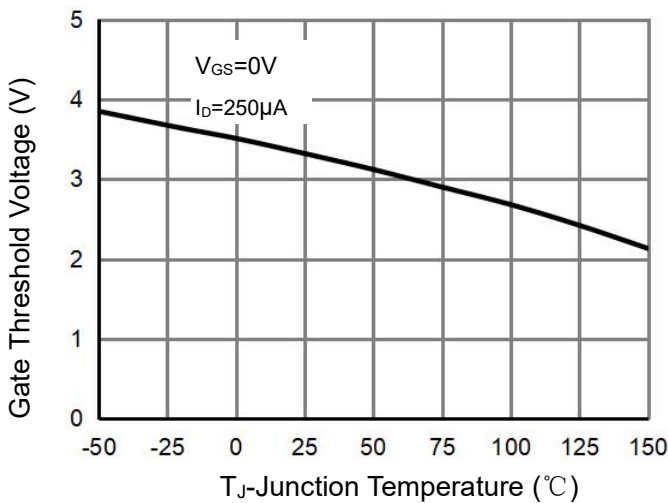


Figure 9 V_{GS(th)}-Junction Temperature

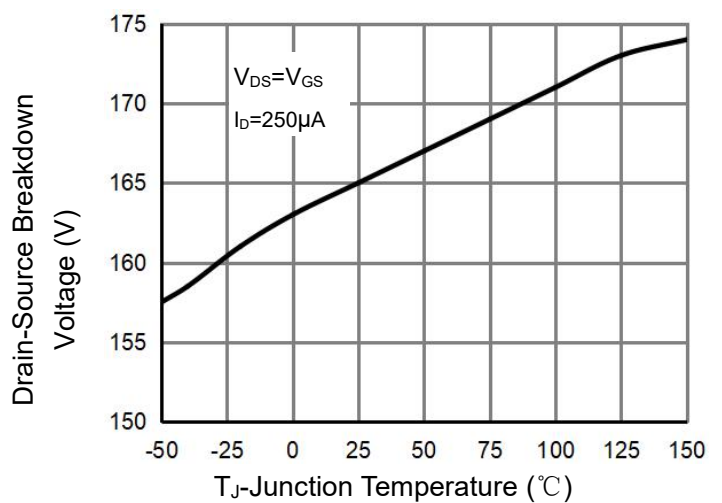


Figure 12 BV_{DSS}-Junction Temperature

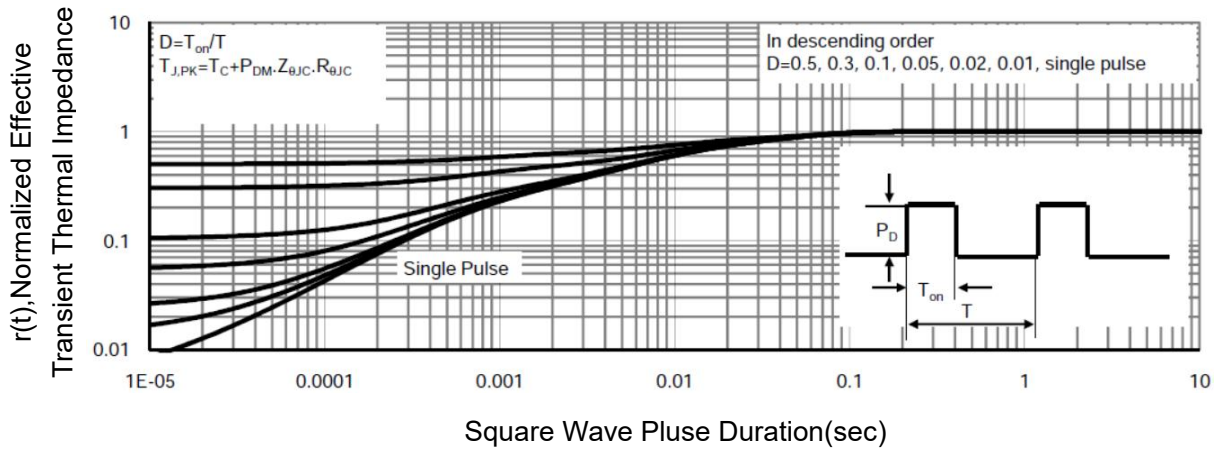
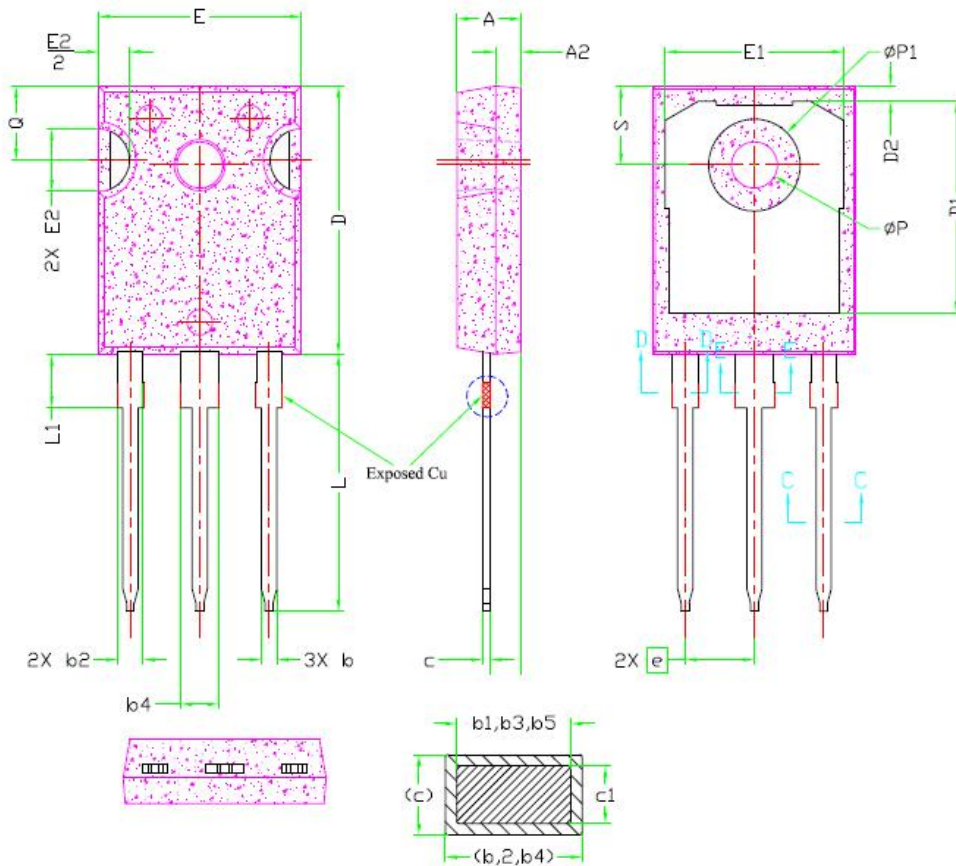


Figure 13 Normalized Maximum Transient Thermal Impedance

TO-247-3L Package Information



SYMBOL	DIMENSIONS			NOTES
	MIN.	NOM.	MAX.	
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.50	2.00	2.49	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.55	0.60	0.69	6
c1	0.55	0.60	0.65	
D	20.80	20.95	21.10	4
D1	16.25	16.55	17.65	5
D2	0.51	1.19	1.35	
E	15.75	15.94	16.13	4
E1	13.46	14.02	14.16	5
E2	4.32	4.91	5.49	3
e	5.44BSC			
L	19.81	20.07	20.32	
L1	4.10	4.19	4.40	6
$\varnothing P$	3.56	3.61	3.65	7
$\varnothing P1$	7.19REF.			
Q	5.39	5.79	6.20	
S	6.04	6.17	6.30	

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