

NCE N-Channel Super Trench II Power MOSFET

Description

The NCEP18N10AQ uses **Super Trench II** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and Q_g . This device is ideal for high-frequency switching and synchronous rectification.

Application

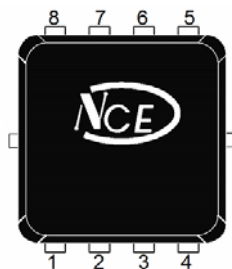
- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

General Features

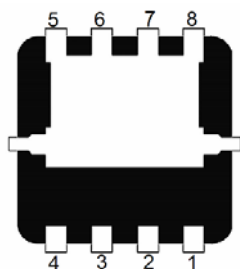
- $V_{DS} = 100V, I_D = 35A$
 $R_{DS(ON)} = 16.0m\Omega$ (typical) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 18.0m\Omega$ (typical) @ $V_{GS} = 4.5V$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)
- Very low on-resistance $R_{DS(on)}$
- 150 °C operating temperature
- Pb-free lead plating

100% UIS TESTED!
100% ΔV_{ds} TESTED!

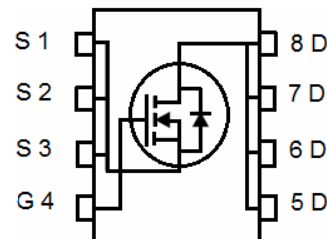
DFN 3.3X3.3



Top View



Bottom View



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP18N10AQ	NCEP18N10AQ	DFN3.3X3.3-8L	-	-	-

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	35	A
Drain Current-Continuous($T_C = 100^\circ C$)	$I_D(100^\circ C)$	25	A
Pulsed Drain Current	I_{DM}	140	A
Maximum Power Dissipation	P_D	48	W
Derating factor		0.39	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	115	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Case ^(Note 2)	$R_{\theta JC}$	2.6	$^\circ C/W$
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Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250μA	100		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.2	1.7	2.2	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =17.5A	-	16	18	mΩ
		V _{GS} =4.5V, I _D =17.5A	-	20	22	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =17.5A	20	-	-	S
Dynamic Characteristics ^(Note4)						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, F=1.0MHz	-	1719.5	-	PF
Output Capacitance	C _{oss}		-	147.4	-	PF
Reverse Transfer Capacitance	C _{rss}		-	16	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =17.5A V _{GS} =10V, R _G =3Ω	-	14	-	nS
Turn-on Rise Time	t _r		-	16	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28	-	nS
Turn-Off Fall Time	t _f		-	8	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =17.5A, V _{GS} =10V	-	37.6	-	nC
Gate-Source Charge	Q _{gs}		-	6.5		nC
Gate-Drain Charge	Q _{gd}		-	9.5		nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V _{SD}	V _{GS} =0V, I _S =17.5A	-		1.2	V
Diode Forward Current ^(Note 2)	I _S		-	-	35	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = 17.5A	-	43	-	nS
Reverse Recovery Charge	Q _{rr}	di/dt = 100A/μs ^(Note3)	-	90	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition : $T_J=25^{\circ}\text{C}, V_{DD}=50V, V_G=10V, L=0.5mH, R_g=25\Omega$

Typical Electrical and Thermal Characteristics

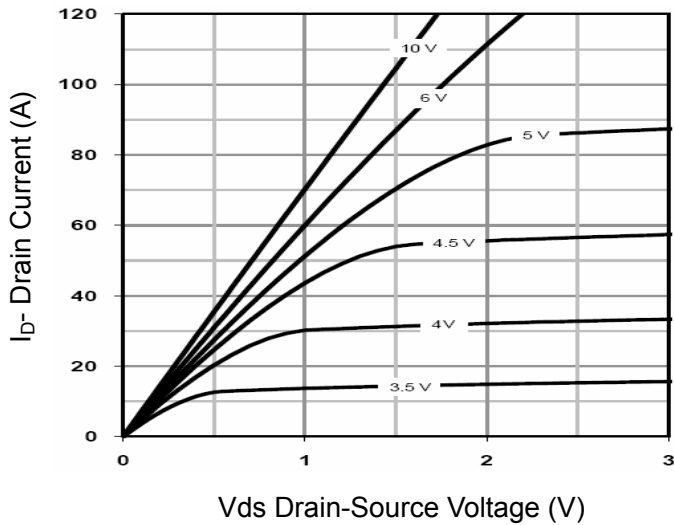


Figure 1 Output Characteristics

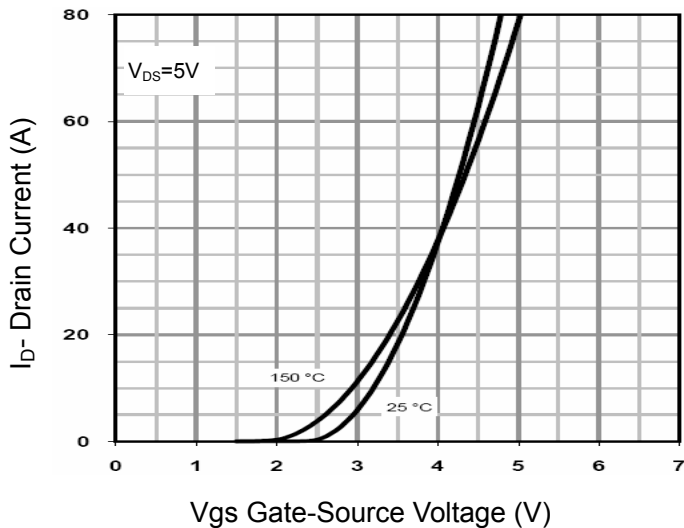


Figure 2 Transfer Characteristics

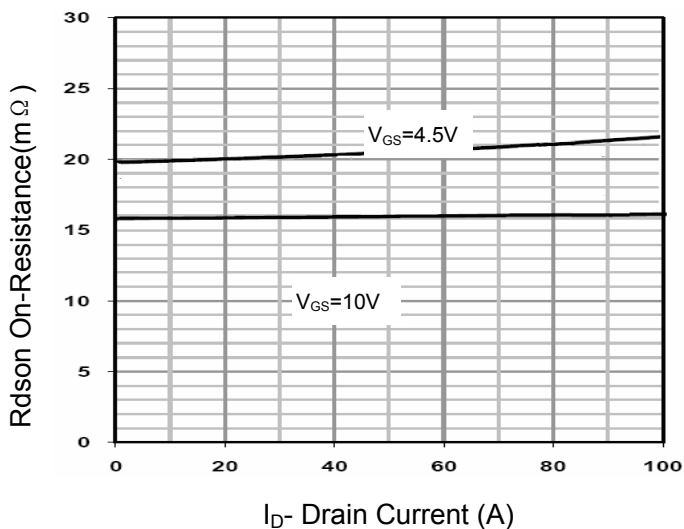


Figure 3 Rdson- Drain Current

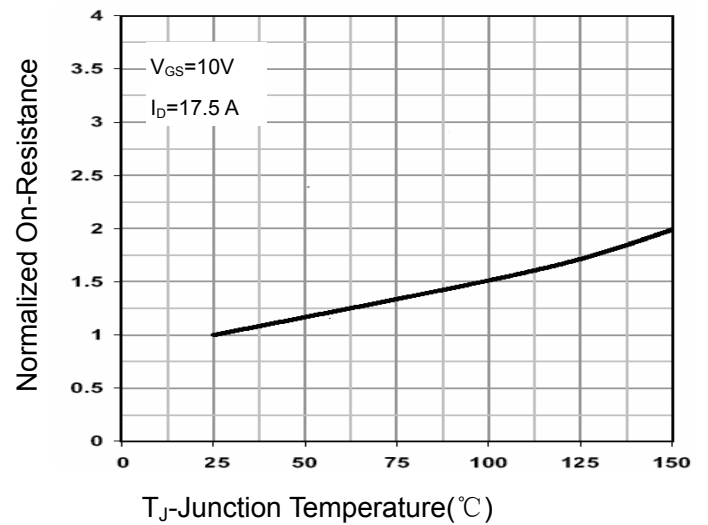


Figure 4 Rdson-Junction Temperature

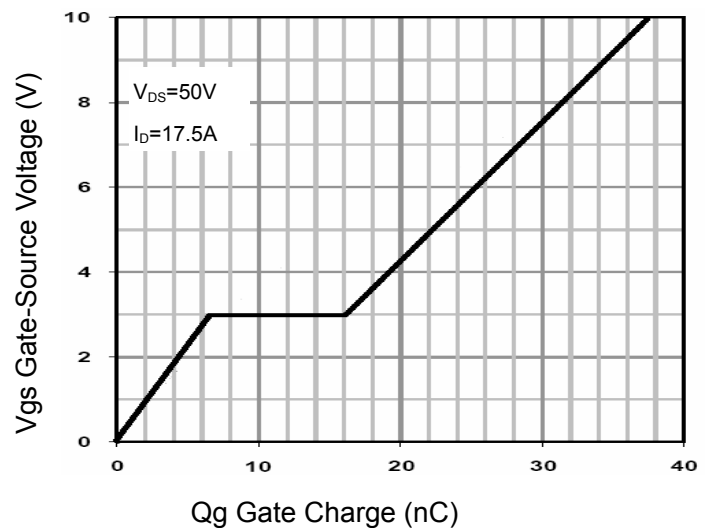


Figure 5 Gate Charge

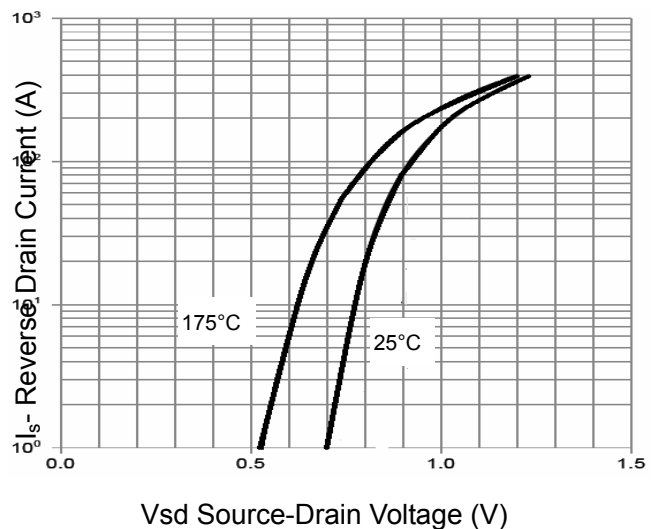
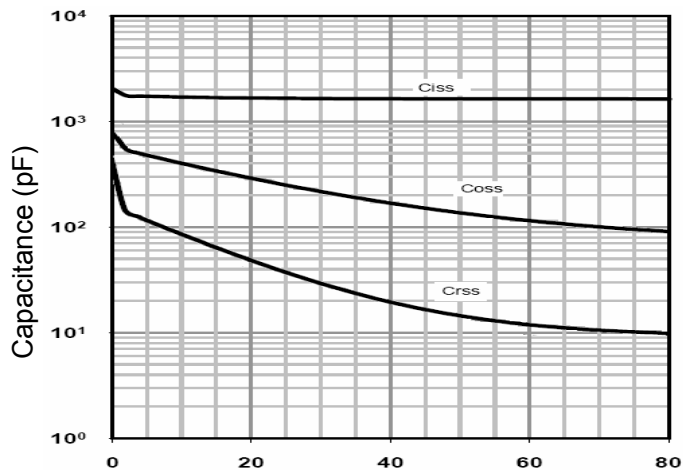
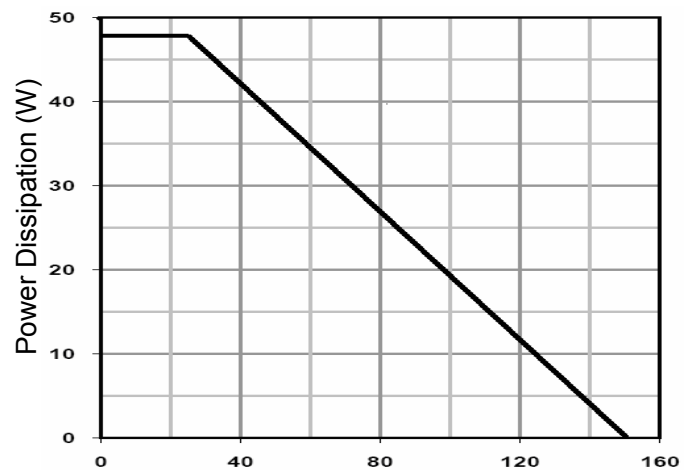


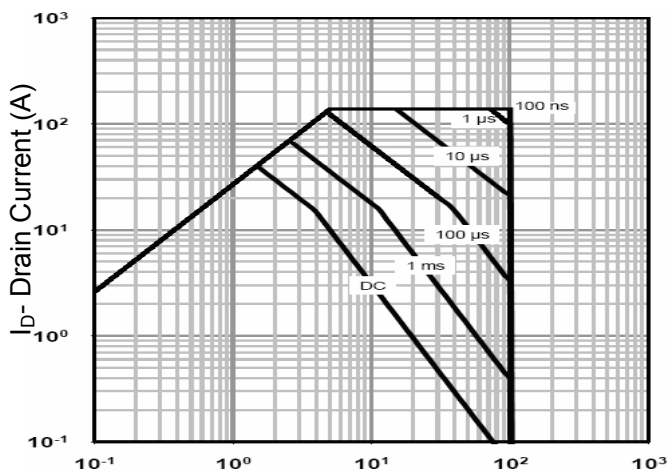
Figure 6 Source- Drain Diode Forward



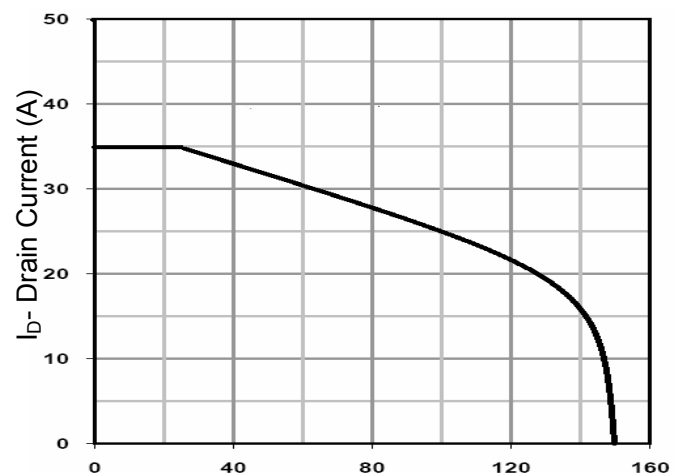
Vds Drain-Source Voltage (V)
Figure 7 Capacitance vs Vds



T_J-Junction Temperature(°C)
Figure 9 Power De-rating



Vds Drain-Source Voltage (V)
Figure 8 Safe Operation Area



T_J-Junction Temperature (°C)
Figure 10 Current De-rating

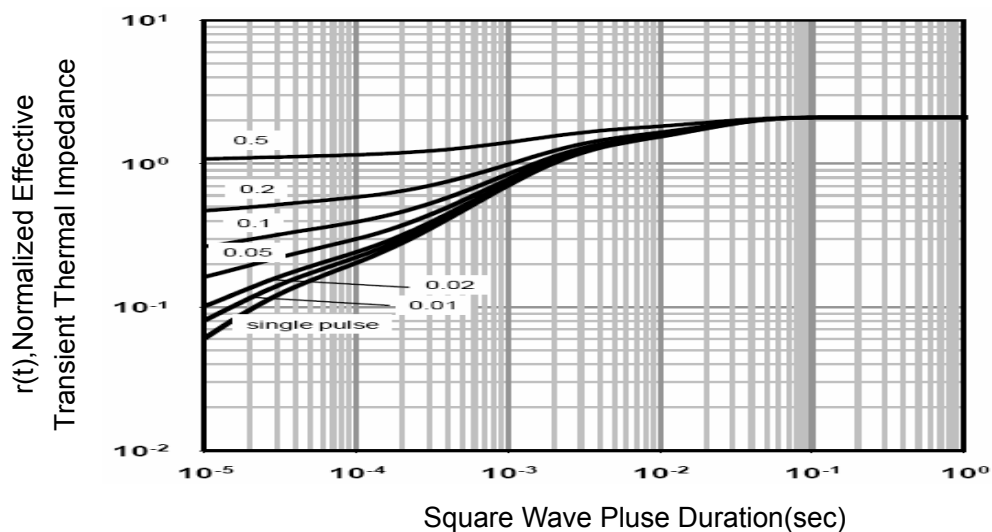
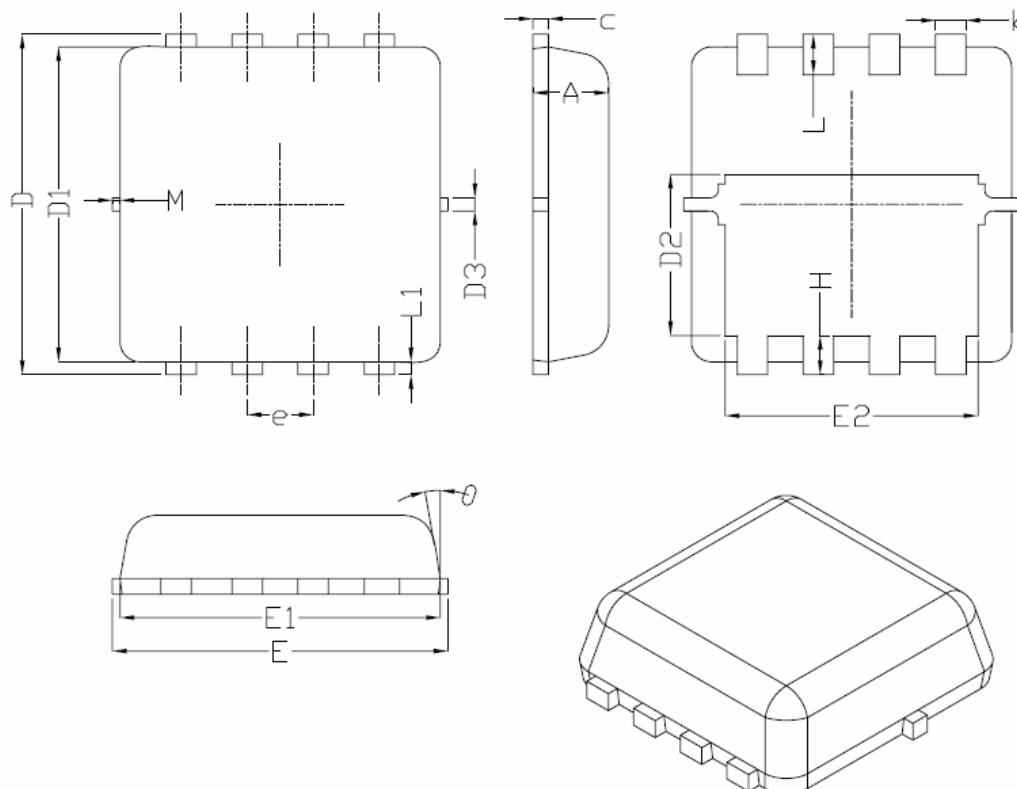


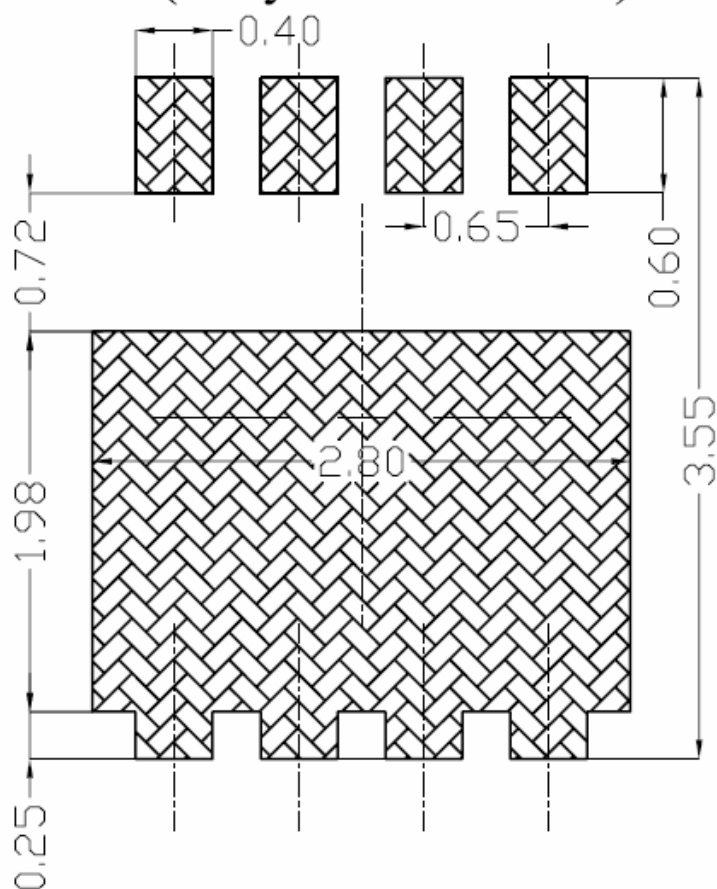
Figure 11 Normalized Maximum Transient Thermal Impedance

DFN3.3X3.3-8L Package Information



Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.48	1.58	1.68
D3	-	0.13	-
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	-	0.13	-
M	*	*	0.15
θ		10°	12°

Land Pattern (Only for Reference)



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