Clock OSC

SG5032CCN

Product name SG5032CCN Product Number / Ordering code

10.000000 MHz HJGA X1G0044710011xx

Please refer to the 8.Packing information about xx (last 2 digits)

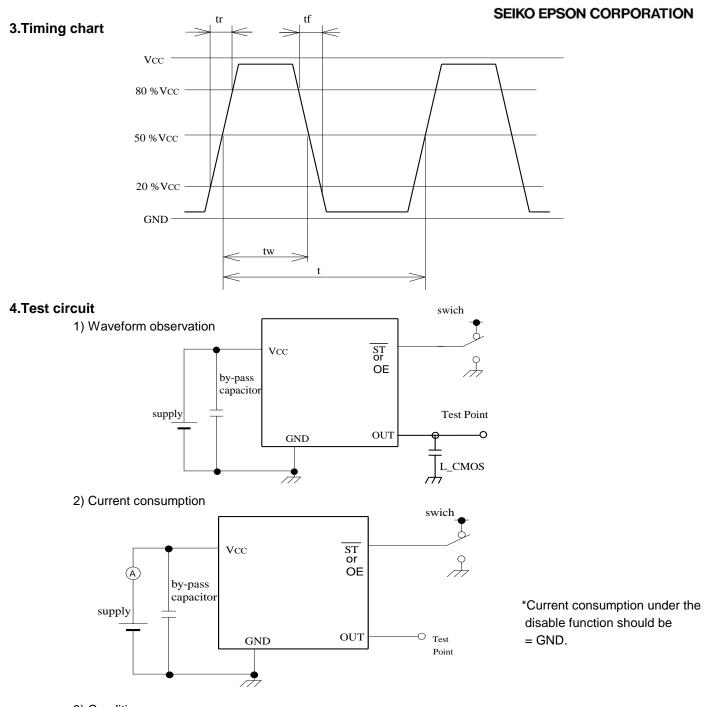
Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 52 mg

1.Absolute maximum ratings	i					
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	7	V	-
Storage temperature	T_stg	-40	-	125	°C	Storage as single product
Input voltage	Vin	-0.5	-	Vcc+0.5	V	OE terminal

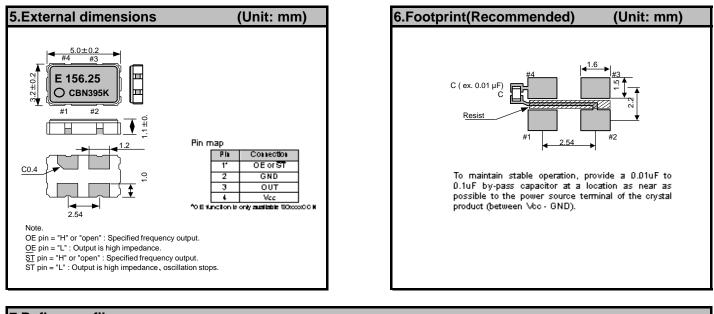
2.Specifications(characteris	stics)					
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Output frequency	fO		10.0000		MHz	
Supply voltage	Vcc	4.5	5	5.5	V	-
Operating temperature	T_use	-40	-	85	°C	-
Frequency tolerance	f_tol	-50	-	50	x10 ⁻⁶	T_use
Current consumption	lcc	-	-	20	mA	No load condition
Stand-by current	I_std	-	-	-	μA	-
Disable current	I_dis	-	-	10.0	mA	OE = GND
Symmetry	SYM	40	-	60	%	50% Vcc Level L_CMOS=<50pF
Output voltage	V _{OH}	Vcc-0.4	-	-		-
	V _{OL}	-	-	0.4		-
Output load condition	L_CMOS	-	-	50	pF	CMOS Load
Input voltage	V _{IH}	0.8Vcc	-	-		OE terminal
	V _{IL}	-	-	0.2Vcc		OE terminal
Rise time	t _r	-	-	5	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=50pF
Fall time	tf	-	-	5	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=50pF
Start-up time	t_str	-	-	5	ms	t = 0 at 0.9Vcc
Jitter	t _{DJ}	-	TBD	-	ps	Deterministic Jitter
	T _{RJ}	-	TBD	-	ps	Random Jitter
	t _{RMS}	-	TBD	-	ps	δ(RMS of total distribution)
	t _{p-p}	-	TBD	-	ps	Peak to Peak
	t _{acc}	-	TBD	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t _{PJ}	-	TBD	-	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	TBD	-	dBc/Hz	Off set 1Hz
		-	TBD	-	dBc/Hz	Off set 10Hz
		-	TBD	-	dBc/Hz	Off set 100Hz
		-	TBD	-	dBc/Hz	Off set 1kHz
		-	TBD	-	dBc/Hz	Off set 10kHz
		-	TBD	-	dBc/Hz	Off set 100kHz
		-	TBD	-	dBc/Hz	Off set 1MHz
Frequency aging	f_age	-5	-	5	x10 ⁻⁶	@+25°C first year
		-	-	-		-

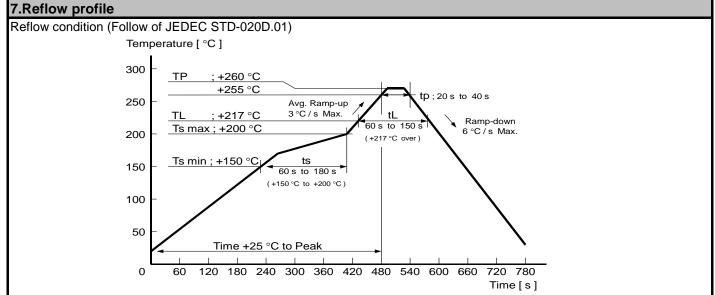


3) Condition

- (1) Oscilloscope
- · Band width should be minimum 5 times higher (wider) than measurement frequency.
- · Probe earth should be placed closely from test point and lead length should be as short as possible
- * Recommendable to use miniature socket. (Don't use earth lead.)
- (2) L_CMOS also includes probe capacitance.
- (3) By-pass capacitor (0.01 mF to 0.1 mF) is placed closely between VCC and GND.
- (4) Use the current meter whose internal impedance value is small.
- (5) Power supply
- \cdot Start up time (0 %VCC \circledast 90 %VCC) of power source should be more than 150 ms.
- \cdot Impedance of power supply should be as lowest as possible.

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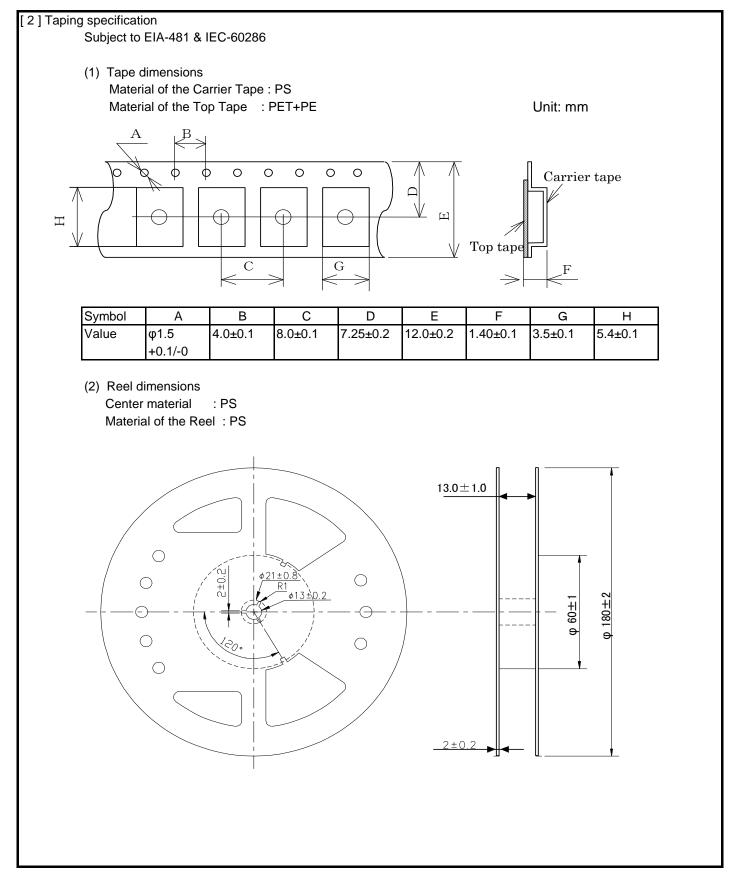




8.Packing information

[1]Produc	t number la	ast 2 digits code(xx) description		The recommended code is "00"
	X1G0044	710011xx		
	Code	Condition	Code	Condition
	01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
	11	Any Q'ty / Reel	00	1000pcs / Reel
	12	250pcs / Reel		

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