

Clock OSC

SG7050CCN

Product name SG7050CCN 8.000000 MHz HJGA

Product Number / Ordering code X1G0045010015xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 147 mg

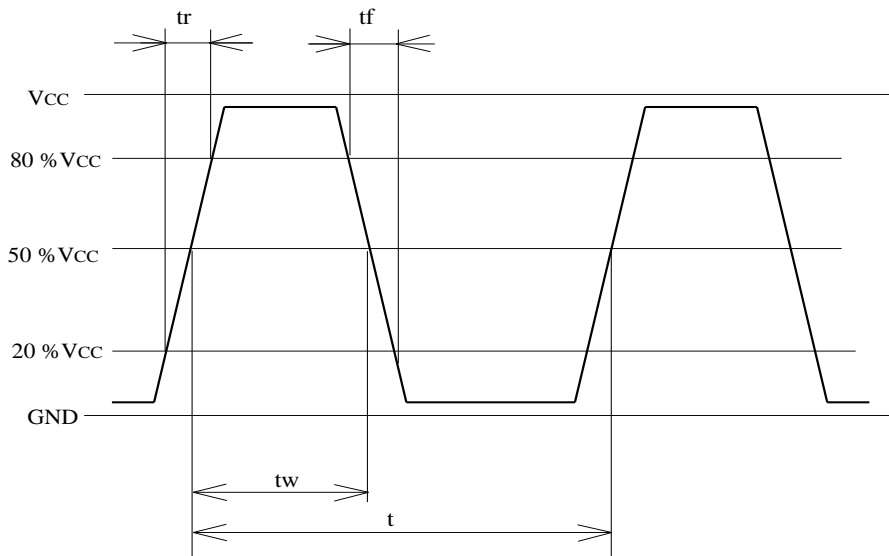
1.Absolute maximum ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|------------------------|----------------------|------|------|----------------------|------|---------------------------|
| Maximum supply voltage | V _{cc} -GND | -0.3 | - | +7 | V | - |
| Storage temperature | T _{stg} | -40 | - | +125 | °C | Storage as single product |
| Input voltage | V _{in} | -0.5 | - | V _{cc} +0.5 | V | OE terminal |

2.Specifications(characteristics)

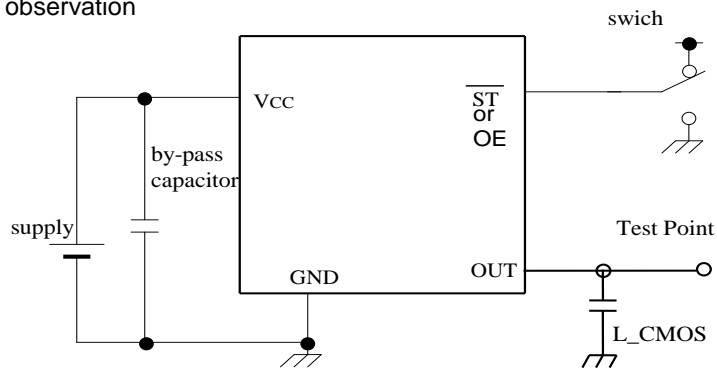
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|-----------------------|-------------------|----------------------|----------|--------------------|-------------------|---|
| Output frequency | f ₀ | | 8.000000 | | MHz | |
| Supply voltage | V _{cc} | 4.5 | 5 | 5.5 | V | - |
| Operating temperature | T _{use} | -40 | - | +85 | °C | - |
| Frequency tolerance | f _{tol} | -50 | - | 50 | x10 ⁻⁶ | T _{use} |
| Current consumption | I _{cc} | - | - | 20 | mA | No load condition |
| Stand-by current | I _{std} | - | - | - | μA | - |
| Disable current | I _{dis} | - | - | 10.0 | mA | OE = GND |
| Symmetry | SYM | 40 | - | 60 | % | 50% V _{cc} Level L _{CMOS} =<50pF |
| Output voltage | V _{OH} | V _{cc} -0.4 | - | - | | - |
| | V _{OL} | - | - | 0.4 | | - |
| Output load condition | L _{CMOS} | - | - | 50 | pF | CMOS Load |
| Input voltage | V _{IH} | 0.8V _{cc} | - | - | | OE terminal |
| | V _{IL} | - | - | 0.2V _{cc} | | OE terminal |
| Rise time | t _r | - | - | 5 | ns | 0.2V _{cc} to 0.8V _{cc} Level, L _{CMOS} =50pF |
| Fall time | t _f | - | - | 5 | ns | 0.2V _{cc} to 0.8V _{cc} Level, L _{CMOS} =50pF |
| Start-up time | t _{str} | - | - | 5 | ms | t = 0 at 0.9V _{cc} |
| Jitter | t _{DJ} | - | 0 | - | ps | Deterministic Jitter |
| | t _{RJ} | - | TBD | - | ps | Random Jitter |
| | t _{RMS} | - | TBD | - | ps | δ(RMS of total distribution) |
| | t _{p-p} | - | TBD | - | ps | Peak to Peak |
| | t _{acc} | - | - | - | ps | Accumulated Jitter(δ) n=2 to 50000 cycles |
| Phase jitter | t _{PJ} | - | TBD | - | ps | Off set Frequency: 12kHz to 20MHz |
| Phase noise | L(f) | - | - | - | dBc/Hz | Off set 1Hz |
| | | - | TBD | - | dBc/Hz | Off set 10Hz |
| | | - | TBD | - | dBc/Hz | Off set 100Hz V _{cc} =3.3V |
| | | - | TBD | - | dBc/Hz | Off set 1kHz |
| | | - | TBD | - | dBc/Hz | Off set 10kHz |
| | | - | TBD | - | dBc/Hz | Off set 100kHz V _{cc} =3.3V |
| | | - | TBD | - | dBc/Hz | Off set 1MHz |
| Frequency aging | f _{age} | -5 | - | 5 | x10 ⁻⁶ | @+25°C first year |
| | | - | - | - | | - |

3. Timing chart

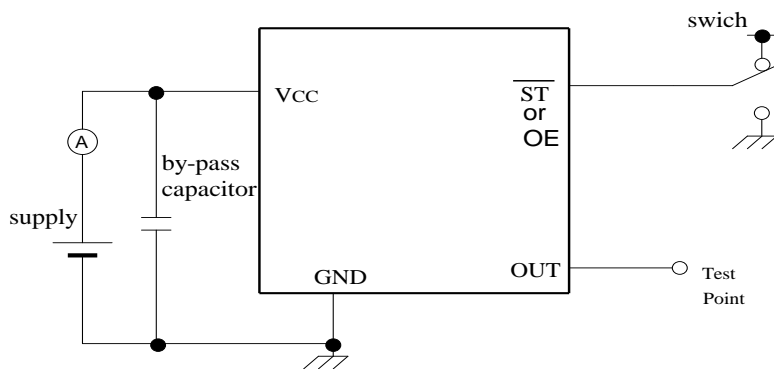


4. Test circuit

1) Waveform observation



2) Current consumption



*Current consumption under the disable function should be = GND.

3) Condition

(1) Oscilloscope

- Band width should be minimum 5 times higher (wider) than measurement frequency.
- Probe earth should be placed closely from test point and lead length should be as short as possible

* Recommendable to use miniature socket. (Don't use earth lead.)

(2) L_CMOS also includes probe capacitance.

(3) By-pass capacitor (0.01 μ F to 0.1 μ F) is placed closely between VCC and GND.

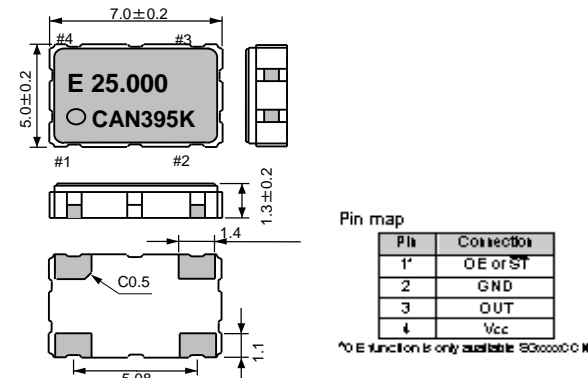
(4) Use the current meter whose internal impedance value is small.

(5) Power supply

- Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 μ s.
- Impedance of power supply should be as lowest as possible.

5.External dimensions

(Unit: mm)



Note.

OE pin = "H" or "open": Specified frequency output.

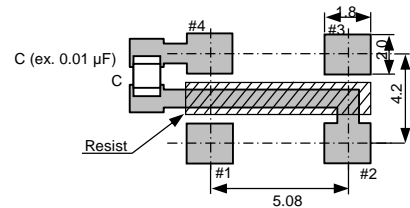
OE pin = "L": Output is high impedance.

ST pin = "H" or "open": Specified frequency output.

ST pin = "L": Output is high impedance, oscillation stops.

6.Footprint(Recommended)

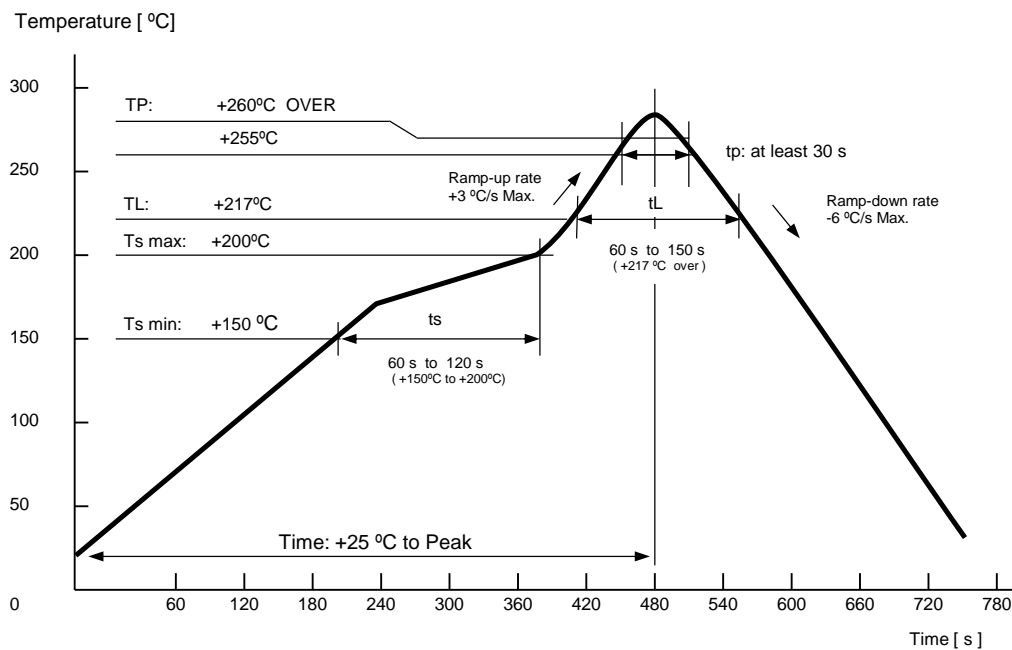
(Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.1)



8.Packing information

| [1] | Product number last 2 digits code(xx) | description |
|-------|---------------------------------------|-------------|
|-------|---------------------------------------|-------------|

The recommended code is "00"

X1G0045010015xx

| Code | Condition | Code | Condition |
|------|------------------------------|------|----------------|
| 01 | Any Q'ty vinyl bag(Tape cut) | 13 | 500pcs / Reel |
| 11 | Any Q'ty / Reel | 00 | 1000pcs / Reel |
| 12 | 250pcs / Reel | | |

[2] Taping specification

Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm



| Symbol | A | B | C | D | E | F |
|--------|------------|---|---|------|----|-----|
| Value | $\phi 1.5$ | 4 | 8 | 9.25 | 16 | 2.3 |

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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