# Clock OSC            SG7050CCN

Product name        SG7050CCN    3.072000  MHz HJGA
Product Number / Ordering code        X1G0045010030xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform   CMOS
Pb free / Complies with EU RoHS directive
Reference weight Typ. 147 mg

## 1.Absolute maximum ratings

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|---|---|---|---|---|---|---|
| Maximum supply voltage | Vcc-GND | -0.3 | - | +7 | V | - |
| Storage temperature | T_stg | -40 | - | +125 | ºC | Storage as single product |
| Input voltage | Vin | -0.5 | - | Vcc+0.5 | V | OE terminal |

## 2.Specifications(characteristics)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions / Remarks |
|---|---|---|---|---|---|---|
| Output frequency | $f_0$ |  | 3.072000 |  | MHz |  |
| Supply voltage | Vcc | 4.5 | 5 | 5.5 | V | - |
| Operating temperature | T_use | -40 | - | +85 | ºC | - |
| Frequency tolerance | f_tol | -50 | - | 50 | $\times 10^{-6}$ | T_use |
| Current consumption | Icc | - | - | 20 | mA | No load condition |
| Stand-by current | I_std | - | - | - | µA | - |
| Disable current | I_dis | - | - | 10.0 | mA | OE = GND |
| Symmetry | SYM | 40 | - | 60 | % | 50% Vcc Level  L_CMOS=<50pF |
| Output voltage | $V_{OH}$ | Vcc-0.4 | - | - |  | - |
|  | $V_{OL}$ | - | - | 0.4 |  | - |
| Output load condition | L_CMOS | - | - | 50 | pF | CMOS Load |
| Input voltage | $V_{IH}$ | 0.8Vcc | - | - |  | OE terminal |
|  | $V_{IL}$ | - | - | 0.2Vcc |  | OE terminal |
| Rise time | $t_r$ | - | - | 5 | ns | 0.2Vcc to 0.8Vcc Level, L_CMOS=50pF |
| Fall time | tf | - | - | 5 | ns | 0.2Vcc to 0.8Vcc Level, L_CMOS=50pF |
| Start-up time | t_str | - | - | 5 | ms | t = 0 at 0.9Vcc |
| Jitter | $t_{DJ}$ | - | 0 | - | ps | Deterministic Jitter |
|  | $t_{RJ}$ | - | TBD | - | ps | Random Jitter |
|  | $t_{RMS}$ | - | TBD | - | ps | δ(RMS of total distribution) |
|  | $t_{p-p}$ | - | TBD | - | ps | Peak to Peak |
|  | $t_{acc}$ | - | - | - | ps | Accumulated Jitter(δ) n=2 to 50000 cycles |
| Phase jitter | $t_{PJ}$ | - | TBD | - | ps | Off set Frequency: 12kHz to 20MHz |
| Phase noise | L(f) | - | - | - | dBc/Hz | Off set 1Hz |
|  |  | - | TBD | - | dBc/Hz | Off set 10Hz |
|  |  | - | TBD | - | dBc/Hz | Off set 100Hz Vcc=3.3V |
|  |  | - | TBD | - | dBc/Hz | Off set 1kHz |
|  |  | - | TBD | - | dBc/Hz | Off set 10kHz |
|  |  | - | TBD | - | dBc/Hz | Off set 100kHz Vcc=3.3V |
|  |  | - | TBD | - | dBc/Hz | Off set 1MHz |
| Frequency aging | f_age | -5 | - | 5 | $\times 10^{-6}$ | @+25ºC first year |
|  |  | - | - | - |  | - |

**3.Timing chart**
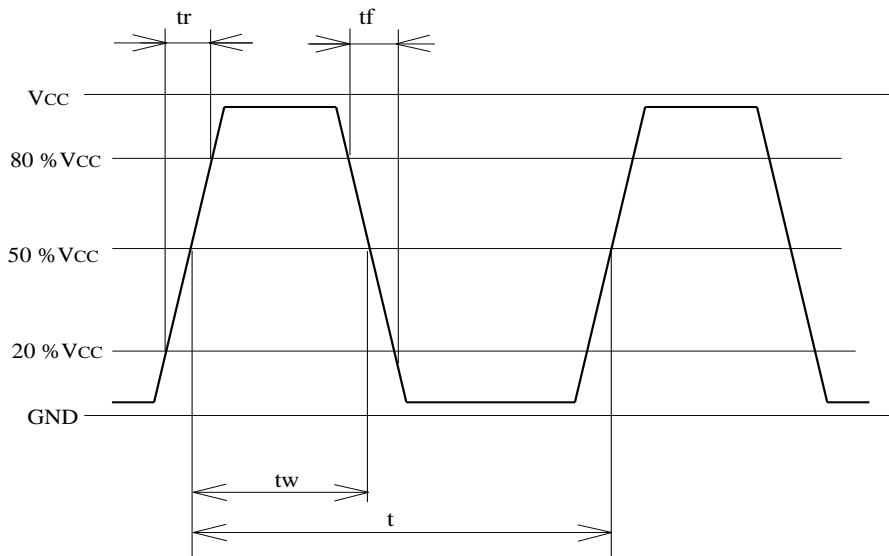


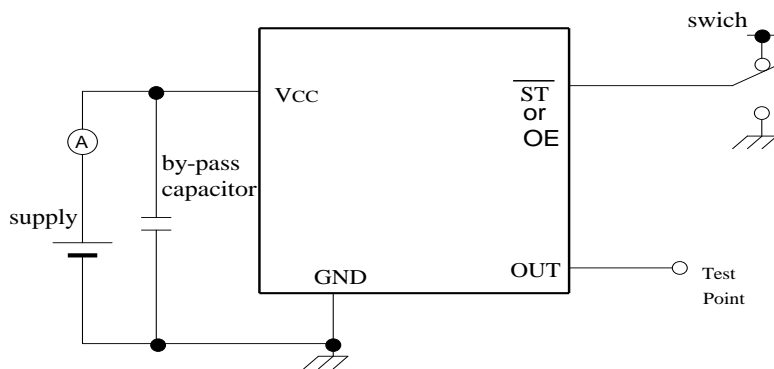**4.Test circuit**

1) Waveform observation
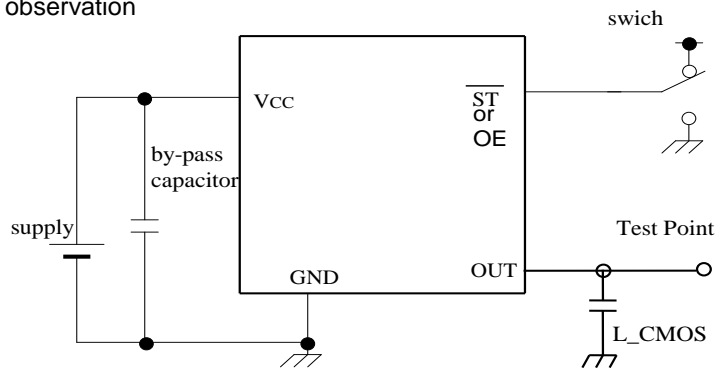


2) Current consumption



*Current consumption under the disable function should be = GND.

3) Condition

(1) Oscilloscope

· Band width should be minimum 5 times higher (wider) than measurement frequency.

· Probe earth should be placed closely from test point and lead length should be as short as possible

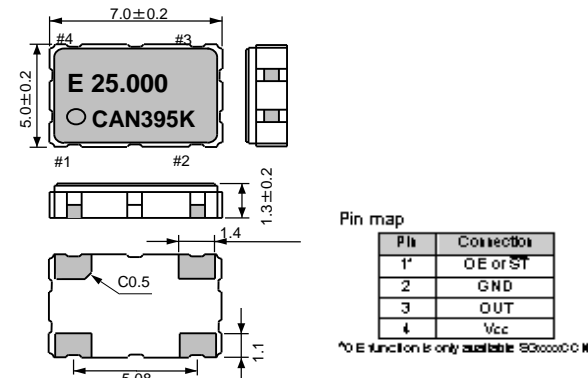* Recommendable to use miniature socket. (Don't use earth lead.)

(2) L_CMOS also includes probe capacitance.

(3) By-pass capacitor (0.01 μF to 0.1 μF) is placed closely between VCC and GND.

(4) Use the current meter whose internal impedance value is small.

(5) Power supply

· Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 μs.

· Impedance of power supply should be as lowest as possible.

## 5.External dimensions (Unit: mm)



7.0±0.2

5.0±0.2

#4 #3

E 25.000
○ CAN395K

#1 #2

1.3±0.2

1.4

C0.5

1.1

5.08

**Pin map**

| Pin | Connection |
|-----|-----------|
| 1* | OE or ST |
| 2 | GND |
| 3 | OUT |
| 4 | Vcc |

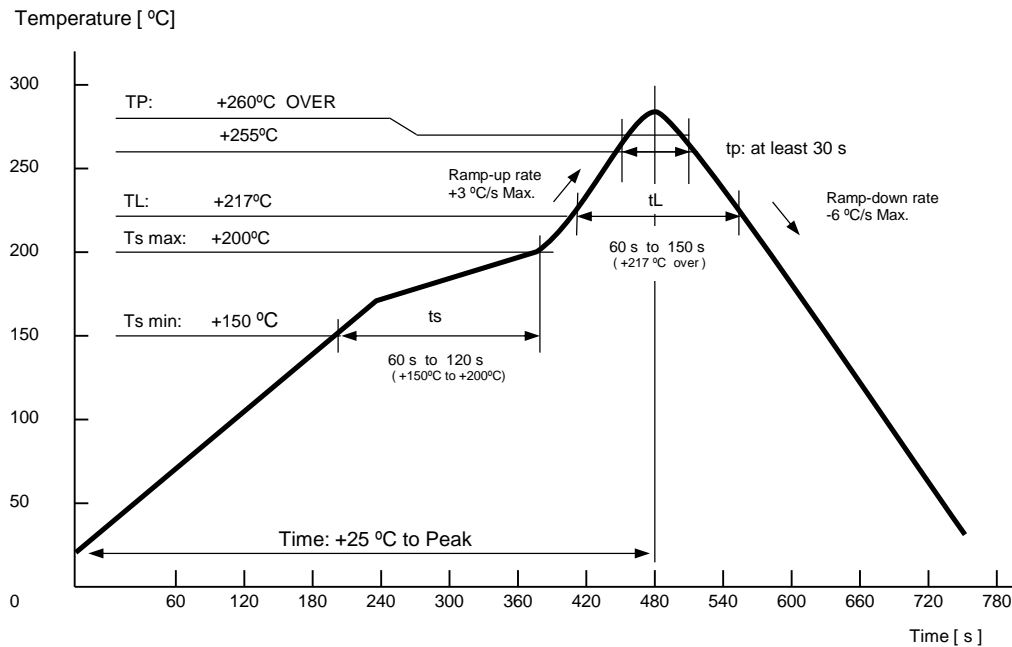*OE function is only available SGxxxxCCN

Note.
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.
ST pin = "H" or "open" : Specified frequency output.
ST pin = "L" : Output is high impedance、oscillation stops.

## 6.Footprint(Recommended) (Unit: mm)



C (ex. 0.01 µF)
C
Resist
#4 #3
#1 #2
.8
2.0
4.2
5.08
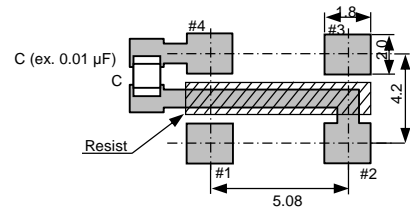
To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

## 7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.1)



Temperature [ ºC]

TP: +260ºC OVER
+255ºC

tp: at least 30 s

Ramp-up rate +3 ºC/s Max.

TL: +217ºC
Ts max: +200ºC

tL

Ramp-down rate -6 ºC/s Max.

60 s to 150 s ( +217 ºC over )

Ts min: +150 ºC

ts

60 s to 120 s ( +150ºC to +200ºC)

Time: +25 ºC to Peak

Time [ s ]

## 8.Packing information

[ 1 ]Product number last 2 digits code(xx) description     The recommended code is "00"

X1G0045010030xx

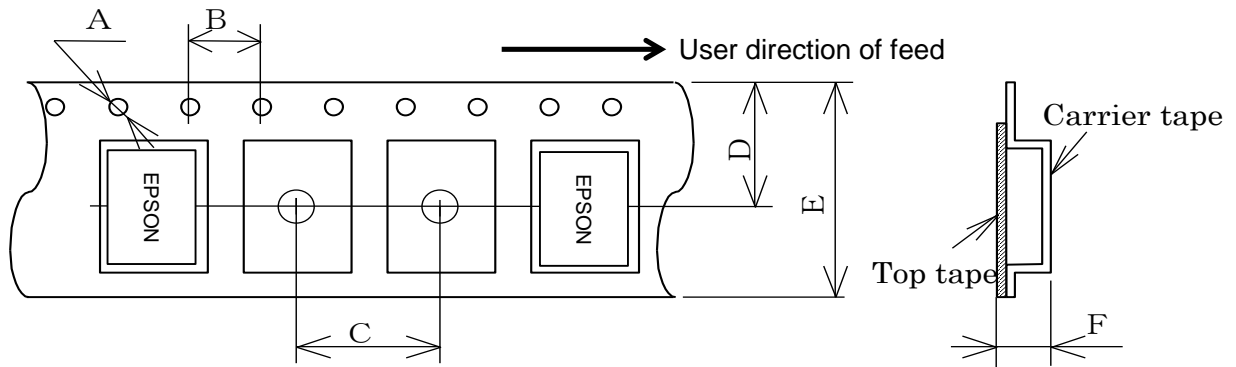| Code | Condition | Code | Condition |
|------|-----------|------|-----------|
| 01 | Any Q'ty vinyl bag(Tape cut) | 13 | 500pcs / Reel |
| 11 | Any Q'ty / Reel | 00 | 1000pcs / Reel |
| 12 | 250pcs / Reel | | |

[ 2 ] Taping specification
Subject to EIA-481 & IEC-60286

(1) Tape dimensions
Material of the Carrier Tape : PS
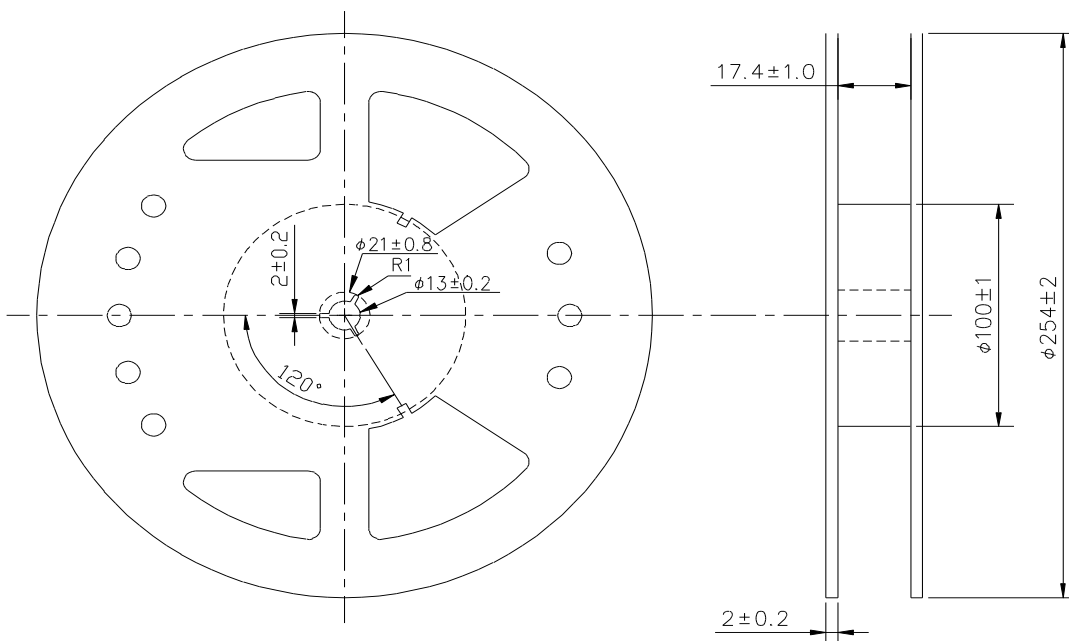Material of the Top Tape : PET+PE

Unit: mm



| Symbol | A | B | C | D | E | F |
|--------|------|---|---|------|----|-----|
| Value | φ1.5 | 4 | 8 | 9.25 | 16 | 2.3 |

(2) Reel dimensions
Center material : PS
Material of the Reel : PS

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