Clock OSC SG7050CCN

Product name SG7050CCN 9.170000 MHz HJGA

Product Number / Ordering code X1G0045010093xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

Pb free / Complies with EU RoHS directive

Reference weight Typ. 147 mg

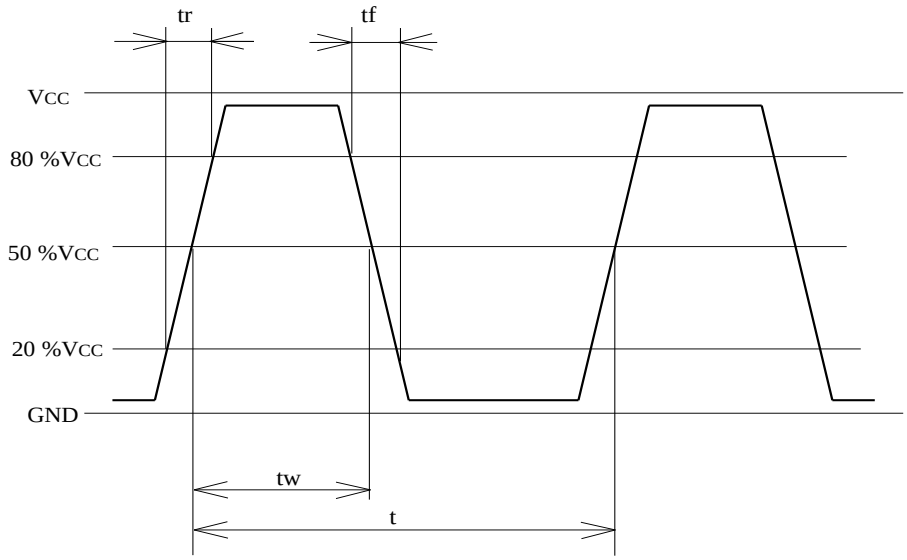
1.Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+7	V	-
Storage temperature	T_stg	-40	-	+125	ºC	Storage as single product
Input voltage	Vin	-0.5	-	Vcc+0.5	V	OE terminal

2.Specifications(characteristics)

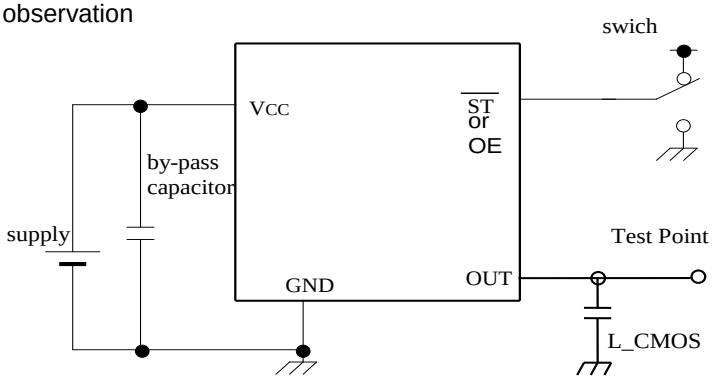
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		9.170000		MHz	
Supply voltage	Vcc	4.5	5	5.5	V	-
Operating temperature	T_use	-40	-	+85	ºC	-
Frequency tolerance	f_tol	-50	-	50	$x10^{-6}$	T_use
Current consumption	Icc	-	-	20	mA	No load condition
Stand-by current	I_std	-	-	-	µA	-
Disable current	I_dis	-	-	10.0	mA	OE = GND
Symmetry	SYM	40	-	60	%	50% Vcc Level L_CMOS=<50pF
Output voltage	V_{OH}	Vcc-0.4	-	-		-
	V_{OL}	-	-	0.4		-
Output load condition	L_CMOS	-	-	50	pF	CMOS Load
Input voltage	V_{IH}	0.8Vcc	-	-		OE terminal
	V_{IL}	-	-	0.2Vcc		OE terminal
Rise time	t_r	-	-	5	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=50pF
Fall time	tf	-	-	5	ns	0.2Vcc to 0.8Vcc Level, L_CMOS=50pF
Start-up time	t_str	-	-	5	ms	t = 0 at 0.9Vcc
Jitter	t_{DJ}	-	-	-	ps	Deterministic Jitter
	t_{RJ}	-	-	-	ps	Random Jitter
	t_{RMS}	-	-	-	ps	σ(RMS of total distribution)
	t_{p-p}	-	-	-	ps	Peak to Peak
	t_{acc}	-	-	-	ps	Accumulated Jitter(σ), n = 2 to 50 000 cycles
Phase jitter	t_{PJ}	-	-	-	ps	Offset Frequency: 12 kHz to 20 MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Offset 1 Hz
		-	-	-	dBc/Hz	Offset 10 Hz
		-	-	-	dBc/Hz	Offset 100 Hz
		-	-	-	dBc/Hz	Offset 1 kHz
		-	-	-	dBc/Hz	Offset 10 kHz, Vcc = 3.3 V
		-	-	-	dBc/Hz	Offset 100 kHz
		-	-	-	dBc/Hz	Offset 1 MHz
Frequency aging	f_age	-5 -	- -	5 -	$x10^{-6}$	@+25ºC first year -

3.Timing chart

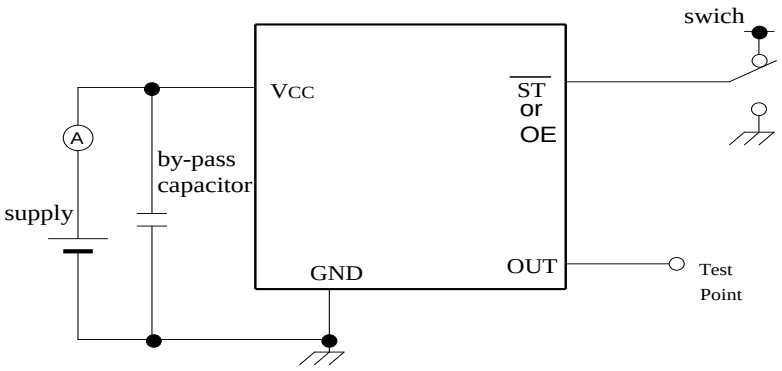


4.Test circuit

1) Waveform observation



2) Current consumption



*Current consumption under the disable function should be = GND.

3) Condition

(1) Oscilloscope

· Band width should be minimum 5 times higher (wider) than measurement frequency.

· Probe earth should be placed closely from test point and lead length should be as short as possible

* Recommendable to use miniature socket. (Don't use earth lead.)

(2) L_CMOS also includes probe capacitance.

(3) By-pass capacitor (0.01 µF to 0.1 µF) is placed closely between VCC and GND.

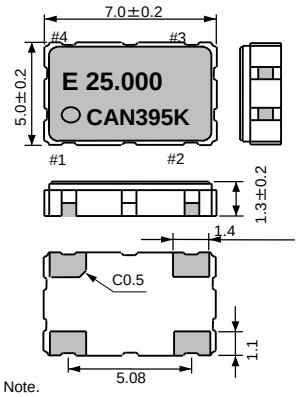
(4) Use the current meter whose internal impedance value is small.

(5) Power supply

· Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 µs.

· Impedance of power supply should be as lowest as possible.

5.External dimensions (Unit: mm)



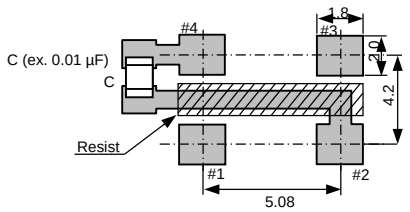
Pin map

Pin	Connection
1*	OE or ST
2	GND
3	OUT
4	Vcc

*) E function is only available SGxxxxCC M

Note.
OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.
ST pin = "H" or "open" : Specified frequency output.
ST pin = "L" : Output is high impedance、oscillation stops.

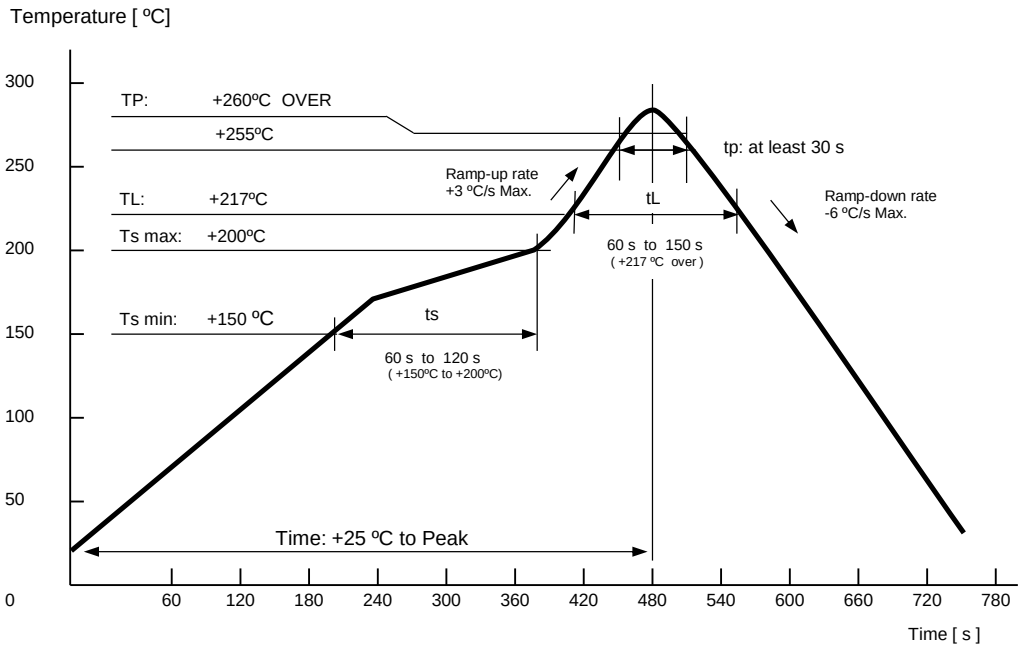
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.1)



8.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1G0045010093xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification

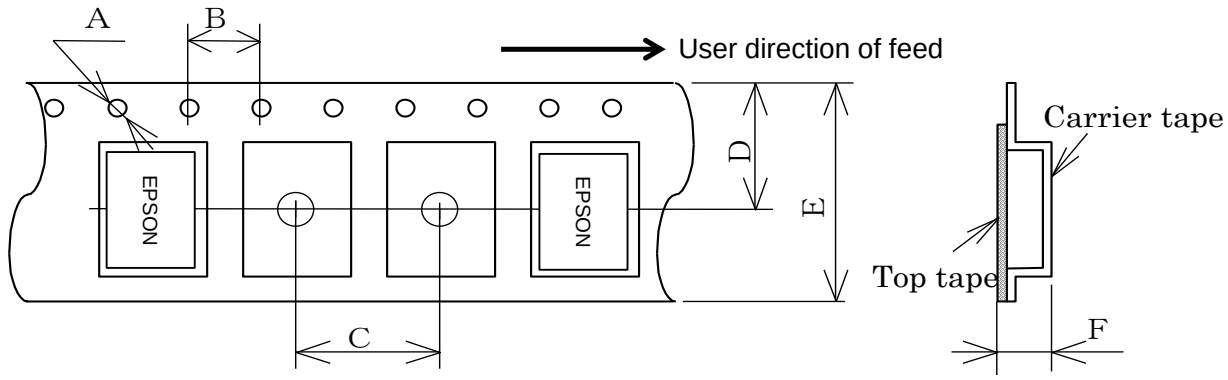
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

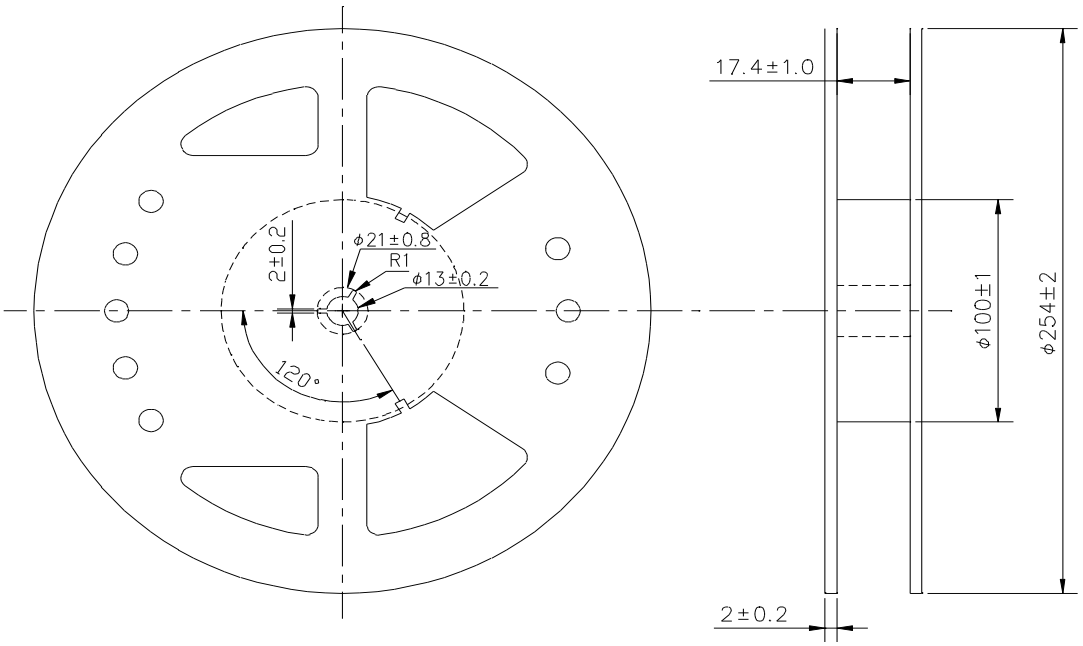


Symbol	A	B	C	D	E	F
Value	φ1.5	4	8	9.25	16	2.3

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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