

Clock OSC

SG7050EAN

Product name SG7050EAN 75.000000 MHz KEGA  
 Product Number / Ordering code X1G0042910030xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 149 mg

**1.Absolute maximum ratings**

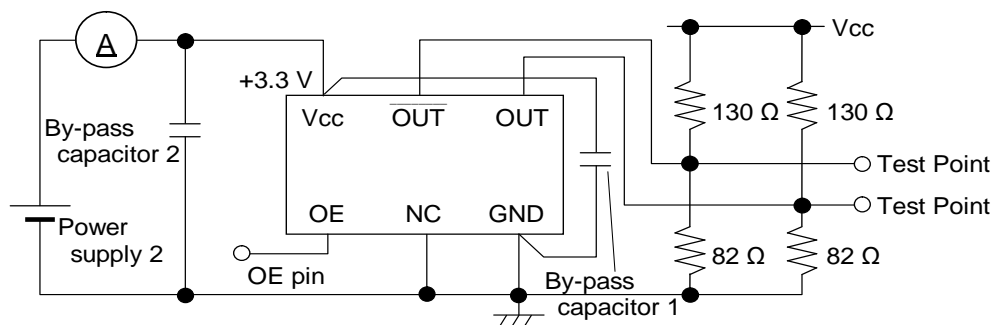
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	V <sub>cc-GND</sub>	-0.3	-	+4	V	-
Storage temperature	T <sub>stg</sub>	-40	-	+125	°C	Storage as single product
Input voltage	V <sub>in</sub>	-0.3	-	V <sub>cc</sub> +0.3	V	ST or OE Terminal

**2.Specifications(characteristics)**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f <sub>0</sub>		75.0000		MHz	
Supply voltage	V <sub>cc</sub>	2.25	-	3.63	V	-
Operating temperature	T <sub>use</sub>	-40	-	+85	°C	-
Frequency tolerance	f <sub>tol</sub>	-30	-	30	x10 <sup>-6</sup>	-
Current consumption	I <sub>cc</sub>	-	-	65	mA	OE = V <sub>cc</sub> , L_ECL = 50 ohm
Stand-by current	I <sub>std</sub>	-	-	-	mA	-
Disable current	I <sub>dis</sub>	-	-	20.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	At output crossing point
Output voltage(LV-PECL)	V <sub>OH</sub>	V <sub>cc</sub> -1.0	-	-	V	-
	V <sub>OL</sub>	-	-	V <sub>cc</sub> -1.62	V	-
Output load condition(ECL)	L_ECL	-	50	-	Ω	Terminated to V <sub>cc</sub> - 2.0V
Input voltage	V <sub>IH</sub>	70% V <sub>cc</sub>	-	-		OE Terminal
	V <sub>IL</sub>	-	-	30% V <sub>cc</sub>		OE Terminal
Rise time	t <sub>r</sub>	-	-	350	ps	At 20% to 80% output swing
Fall time	t <sub>f</sub>	-	-	350	ps	At 20% to 80% output swing
Start-up time	t <sub>str</sub>	-	-	3	ms	-
Jitter	t <sub>DJ</sub>	-	11.6	-	ps	Deterministic Jitter V <sub>cc</sub> =2.5V
	T <sub>RJ</sub>	-	1.1	-	ps	Random Jitter V <sub>cc</sub> =2.5V
	t <sub>RMS</sub>	-	1.8	-	ps	δ(RMS of total distribution) V <sub>cc</sub> =2.5V
	t <sub>p-p</sub>	-	13	-	ps	Peak to Peak V <sub>cc</sub> =2.5V
	t <sub>acc</sub>	-	1.3	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles V <sub>cc</sub> =2.5V
Phase jitter	t <sub>pJ</sub>	-	0.32	-	ps	Offset Frequency: 12kHz to 20MHz V <sub>cc</sub> =2.5V
Phase noise	L(f)	-	-57	-	dBc/Hz	Offset 1Hz V <sub>cc</sub> =2.5V
		-	-89	-	dBc/Hz	Offset 10Hz V <sub>cc</sub> =2.5V
		-	-115	-	dBc/Hz	Offset 100Hz V <sub>cc</sub> =2.5V
		-	-128	-	dBc/Hz	Offset 1kHz V <sub>cc</sub> =2.5V
		-	-137	-	dBc/Hz	Offset 10kHz V <sub>cc</sub> =2.5V
		-	-143	-	dBc/Hz	Offset 100kHz V <sub>cc</sub> =2.5V
		-	-144	-	dBc/Hz	Offset 1MHz V <sub>cc</sub> =2.5V
Frequency aging	f <sub>age</sub>	-5	-	5	x10 <sup>-6</sup> /Year	@ +25°C first year

### 3. Test circuit

1) To observe waveform and current (case 1)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

\* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



\* The lines from OUT and  $\overline{\text{OUT}}$  pin are same length.

\* To measure the disable current, OE pin is connected to GND

3) Measurement condition

A) Oscilloscope

- Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01  $\mu\text{F}$  to 0.1  $\mu\text{F}$ ) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10  $\mu\text{F}$ ) places closely between power supply terminals on the board.

D) Use the current meter whose internal impedance value is small.

E) Power supply

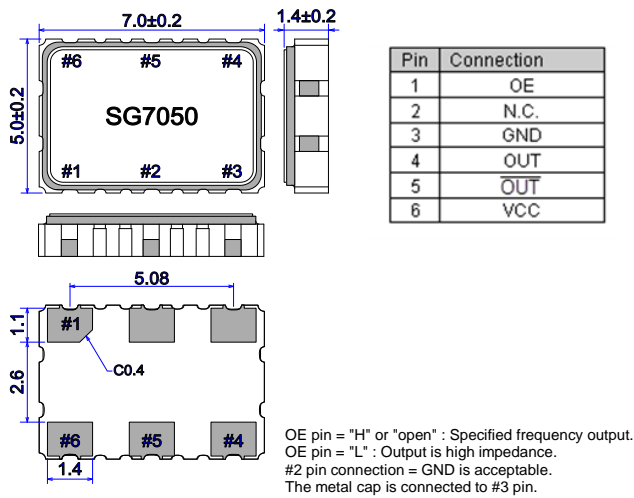
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu\text{s}$  and slew rate should be less than 19.8 mV/ $\mu\text{s}$ .
- Impedance of power supply should be as low as possible.

4.Timing chart



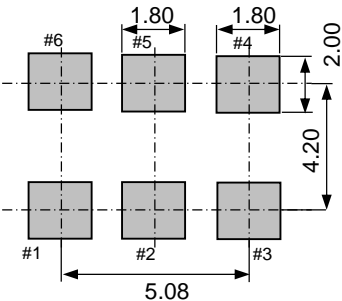
5.External dimensions

(Unit: mm)



6.Footprint(Recommended)

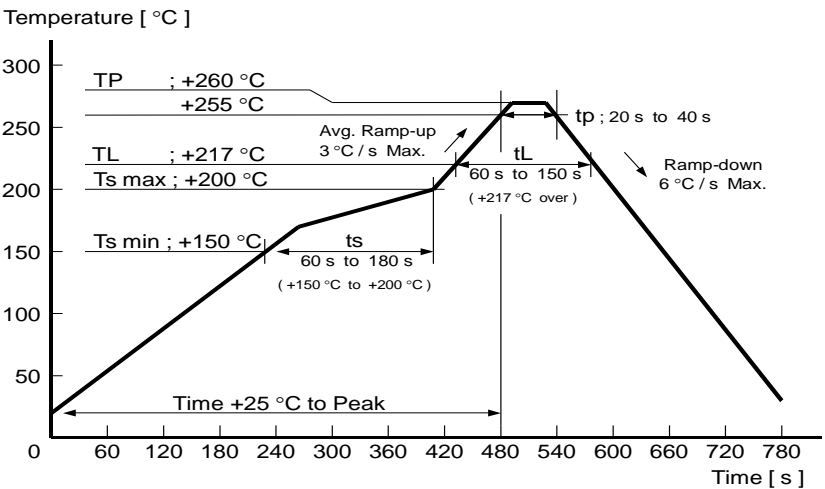
(Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



## 8.Example of schematic layout

This figure shows an example of this product's application schematic.

As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.





- \* By-pass capacitor (approx. 0.01 μF to 0.1 μF) places closely between V<sub>CC</sub> and GND.
- \* By-pass capacitor (approx. 10 μF) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
- \* Terminators place near the input device.

## 9. Packing information

[ 1 ] Product number last 2 digits code(xx) description

The recommended code is "00"

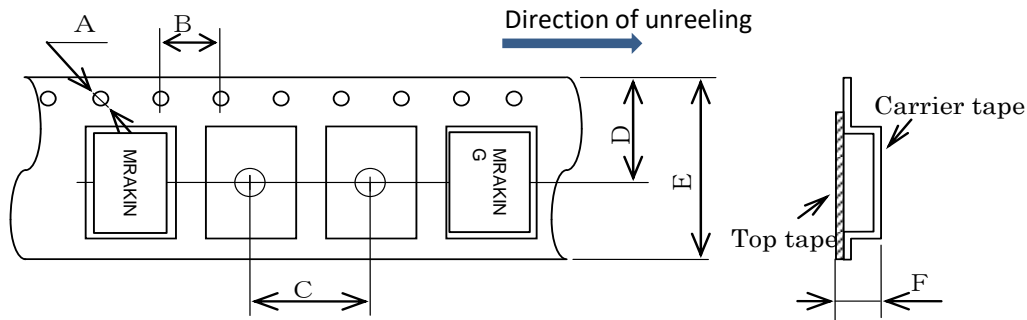
X1G0042910030xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[ 2 ] Taping specification  
Subject to EIA-481 & IEC-60286

- (1) Tape dimensions  
Material of the Carrier Tape : PS  
Material of the Top Tape : PET+PE

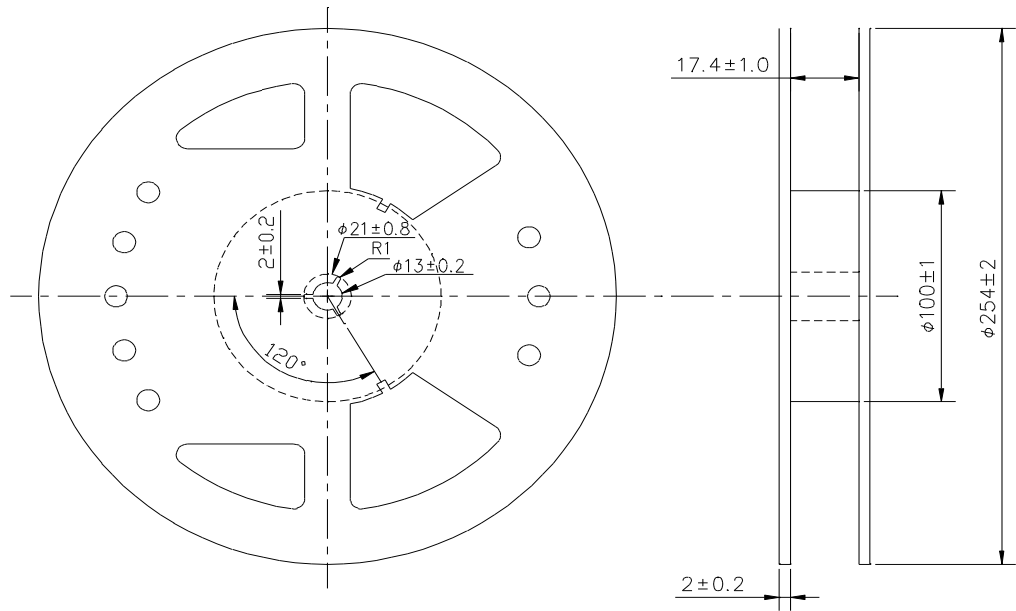
Unit: mm



Symbol	A	B	C	D	E	F
Value	$\phi 1.5$	4	8	9.25	16	2.3

- (2) Reel dimensions  
Center material : PS  
Material of the Reel : PS

Unit: mm



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