# Clock OSC

# SG7050EAN

Product name SG7050EAN 121.500000MHz KEGA
Product Number / Ordering code X1G0042910142xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL Pb free / Complies with EU RoHS directive

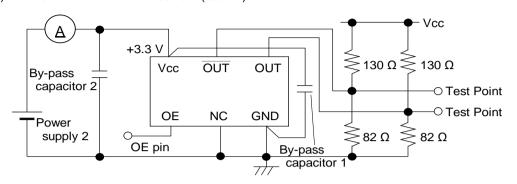
Reference weight Typ. 149 mg

1.Absolute maximum ratings							
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks	
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	0	
Storage temperature	T_stg	-40	-	+125	°C	Storage as single product	
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST or OE Terminal	

2.Specifications(characte	ristics)					
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Output frequency	f0		121.5000		MHz	
Supply voltage	Vcc	2.25	-	3.63	V	-
Operating temperature	T_use	-40	-	+85	°C	-
Frequency tolerance	f_tol	-30	-	30	x10 <sup>-6</sup>	-
Current consumption	Icc	-	-	65	mA	OE = Vcc , L_ECL = 50 ohm
Stand-by current	l_std	-	-	-	mA	-
Disable current	l_dis	-	-	20.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	At output crossing point
Output voltage(LV-PECL)	V <sub>OH</sub>	Vcc-1.0	-	-	V	-
	V <sub>OL</sub>	-	-	Vcc-1.62	V	-
Output load condition(ECL)	L_ECL	-	50	-	Ω	Terminated to Vcc - 2.0V
Input voltage	$V_{IH}$	70% Vcc	-	-		OE Terminal
	$V_{IL}$	-	-	30% Vcc		OE Terminal
Rise time	t <sub>r</sub>	-	-	350	ps	At 20% to 80% output swing
Fall time	tf	-	-	350	ps	At 20% to 80% output swing
Start-up time	t_str	-	-	3	ms	-
Jitter	t <sub>DJ</sub>	-	20	-	ps	Deterministic Jitter Vcc=2.5V
	$T_{RJ}$	-	0.9	-	ps	Random Jitter Vcc=2.5V
	t <sub>RMS</sub>	-	5.5	-	ps	δ(RMS of total distribution) Vcc=2.5V
	t <sub>p-p</sub>	-	24.5	-	ps	Peak to Peak Vcc=2.5V
	t <sub>acc</sub>	-	1.3	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles Vcc=2.5V
Phase jitter	t <sub>PJ</sub>	-	0.33	-	ps	Offset Frequency: 12kHz to 20MHz Vcc=2.5V
Phase noise	L(f)	-	-39	-	dBc/Hz	Offset 1Hz Vcc=2.5V
		-	-74	-	dBc/Hz	Offset 10Hz Vcc=2.5V
		-	-106	-	dBc/Hz	Offset 100Hz Vcc=2.5V
		-	-124	-	dBc/Hz	Offset 1kHz Vcc=2.5V
		-	-133	-	dBc/Hz	Offset 10kHz Vcc=2.5V
		-	-138	-	dBc/Hz	Offset 100kHz Vcc=2.5V
		-	-139	-	dBc/Hz	Offset 1MHz Vcc=2.5V
Frequency aging	f_age	-5	-	5	x10 <sup>-6</sup> /Year	@+25°C first year

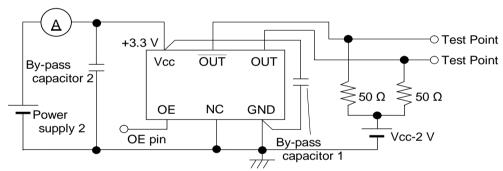
#### 3.Test circuit

1) To observe waveform and current (case 1)



- \* The lines from OUT and OUT pin are same length.
- \* To measure the disable current, OE pin is connected to GND

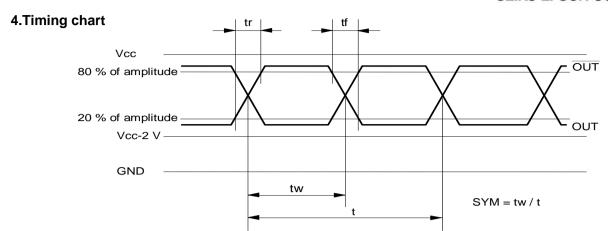
### 2) To observe waveform and current (case 2)

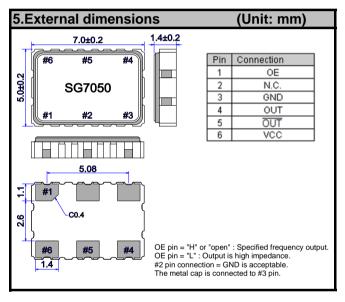


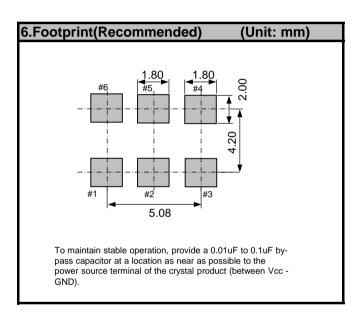
- \* The lines from OUT and OUT pin are same length.
- \* To measure the disable current, OE pin is connected to GND

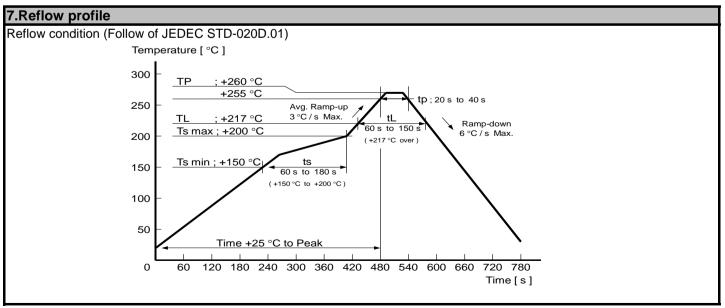
#### 3) Measurement condition

- A) Oscilloscope
- •Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- •Probe ground should be placed closely from test point and lead length should be as short as possible.
- B) By-pass capacitor 1 (approx. 0.01 μF to 0.1 μF) places closely between Vcc and GND.
- C) By-pass capacitor 2 (approx. 10 µF) places closely between power supply terminals on the board.
- D) Use the current meter whose internal impedance value is small.
- E) Power supply
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu$ s and slew rate should be less than 19.8 mV/ $\mu$ s.
- Impedance of power supply should be as low as possible.







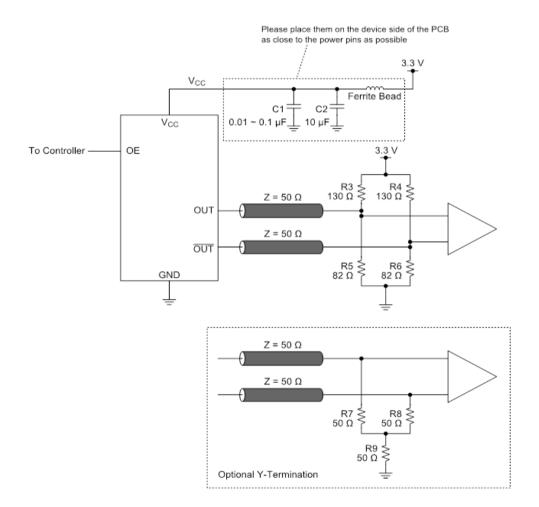


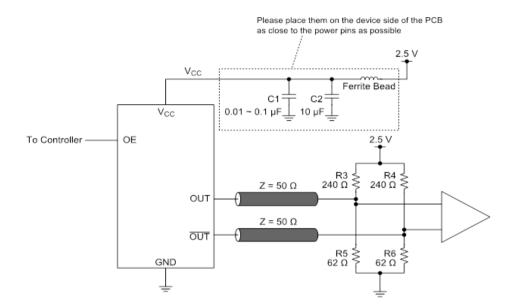
# 8.Example of schematic layout

This figure shows an example of this product's application schematic.

As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.





- \* By-pass capacitor (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.
- \* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance 50  $\Omega$  and same length, and try to make the output lines as short as possible.
- \* Terminators place near the input device.

9.Packing	).Packing information						
[1]Produc	[1] Product number last 2 digits code(xx) description The recommended code is "00"						
	Code	Condition	Code	Condition			
	01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel			
	11	Any Q'ty / Reel	00	1000pcs / Reel			
	12	250pcs / Reel					

# [2] Taping specification

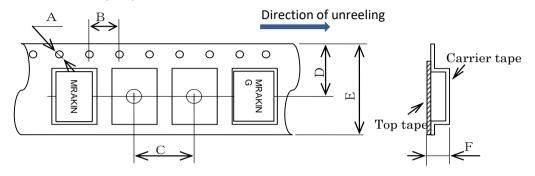
Subject to EIA-481 & IEC-60286

# (1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

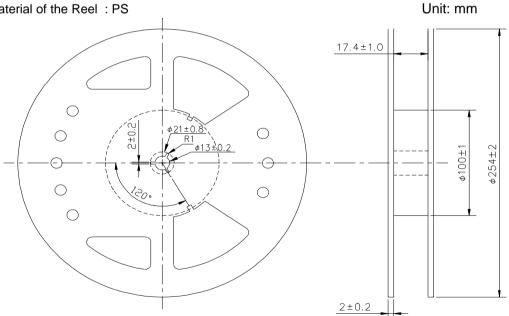
Unit: mm



Sy	/mbol	Α	В	С	D	Е	F
V	alue	φ1.5	4	8	9.25	16	2.3

# (2) Reel dimensions

Center material : PS Material of the Reel : PS



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