Clock OSC SG7050VAN

SEIKO EPSON CORPORATION

Product name SG7050VAN 312.515625MHz KJGA
Product Number / Ordering code X1G0042810016xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LVDS
Pb free / Complies with EU RoHS directive
Reference weight Typ. 149 mg

1.Absolute maximum ratings

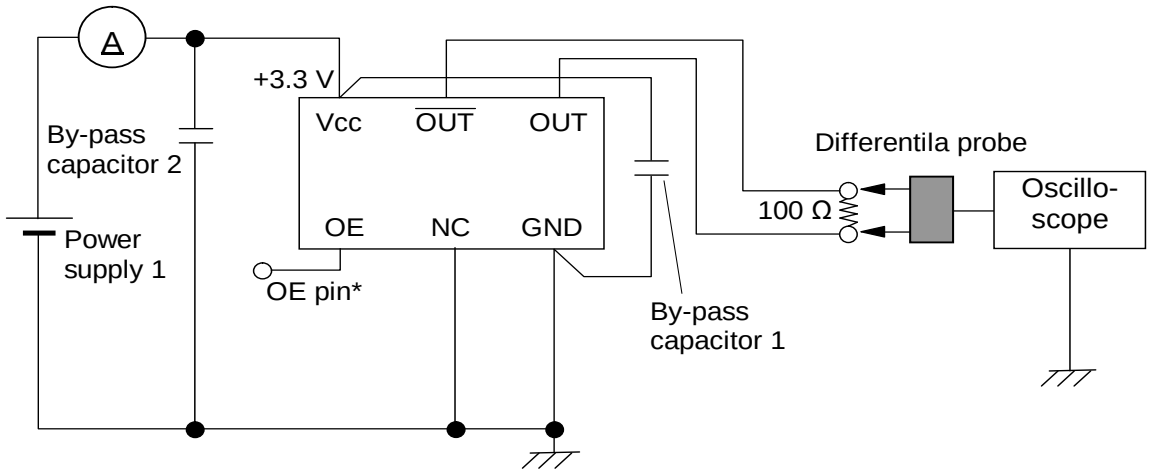
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-
Storage temperature	T_stg	-40	-	+125	ºC	Storage as single product
Input voltage	Vin	-0.3	-	Vcc+0.3	V	OE Terminal

2.Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0	-	312.5156	-	MHz	
Supply voltage	Vcc	2.25	-	3.63	V	-
Operating temperature	T_use	-40	-	+85	ºC	-
Frequency tolerance	f_tol	-50	-	50	$x10^{-6}$	-
Current consumption	Icc	-	-	30	mA	OE = Vcc, L_LVDS = 100 Ω
Stand-by current	I_std	-	-	-	mA	-
Disable current	I_dis	-	-	20.0	mA	OE = GND
Symmetry	SYM	45	-	55	%	At output crossing point
Output voltage(LVDS)	V_{OD}	250	-	450	mV	-
	dV_{OD}	-	-	50	mV	-
	Vos	1.15	-	1.35	V	-
	dVos	-	-	150	mV	-
Output load condition(LVDS)	L_LVDS	-	100	-	Ω	Connected between OUT and $\overline{OUT}$
Input voltage	V_{IH}	70 % Vcc	-	-		-
	V_{IL}	-	-	30 % Vcc		-
Rise time	t_r	-	-	300	ps	-
Fall time	tf	-	-	300	ps	-
Start-up time	t_str	-	-	3	ms	-
Jitter	t_{DJ}	-	12.1	-	ps	Deterministic Jitter Vcc=2.5V
	T_{RJ}	-	1	-	ps	Random Jitter Vcc=2.5V
	t_{RMS}	-	2.4	-	ps	δ(RMS of total distribution) Vcc=2.5V
	t_{p-p}	-	14.3	-	ps	Peak to Peak Vcc=2.5V
	t_{acc}	-	1	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles Vcc=2.5V
Phase jitter	t_{PJ}	-	0.3	-	ps	Offset Frequency: 12kHz to 20MHz Vcc=2.5V
Phase noise	L(f)	-	-35	-	dBc/Hz	Offset 1Hz Vcc=2.5V
		-	-67	-	dBc/Hz	Offset 10Hz Vcc=2.5V
		-	-97	-	dBc/Hz	Offset 100Hz Vcc=2.5V
		-	-1138	-	dBc/Hz	Offset 1kHz Vcc=2.5V
		-	-123	-	dBc/Hz	Offset 10kHz Vcc=2.5V
		-	-129	-	dBc/Hz	Offset 100kHz Vcc=2.5V
		-	-128	-	dBc/Hz	Offset 1MHz Vcc=2.5V
Frequency aging	f_age	-5	-	5	$x10^{-6}$/Year	25 °C, 1st year
		-	-	-		-

3.Test circuit

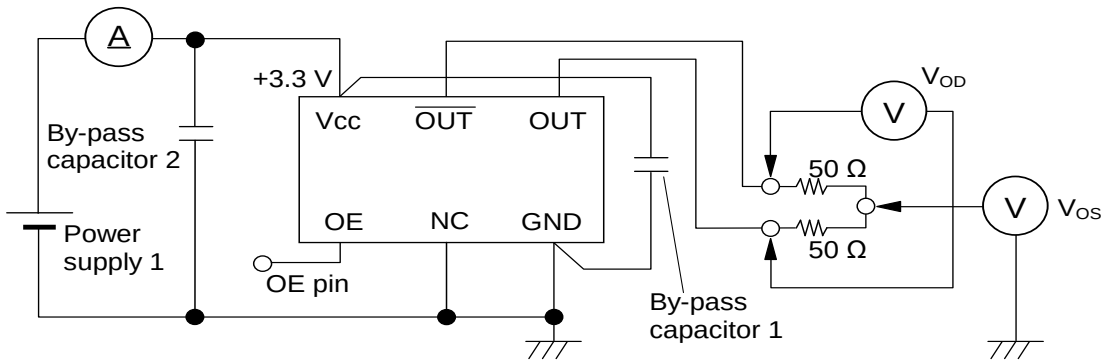
1) To observe waveform and current (case 1)



* The lines from OUT and $\overline{OUT}$ pin are same length.

* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



* The lines from OUT and $\overline{OUT}$ pin are same length.

3) Measurement condition

A) Oscilloscope

•Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).

•Probe ground should be placed closely from test point and lead length should be as short as possible.

B) By-pass capacitor 1 (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10 µF) places closely between power supply terminals on the board.

D) Use the current meter whose internal impedance value is small.

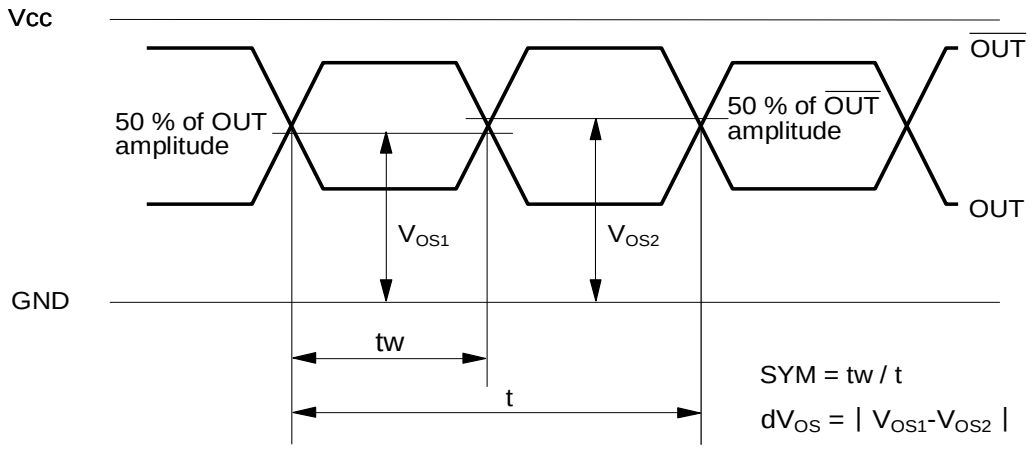
E) Power supply

• Start up time (0 Vg90 %Vcc) of power source should be more than 150 µs and slew rate should be less than 19.8 mV/µs.

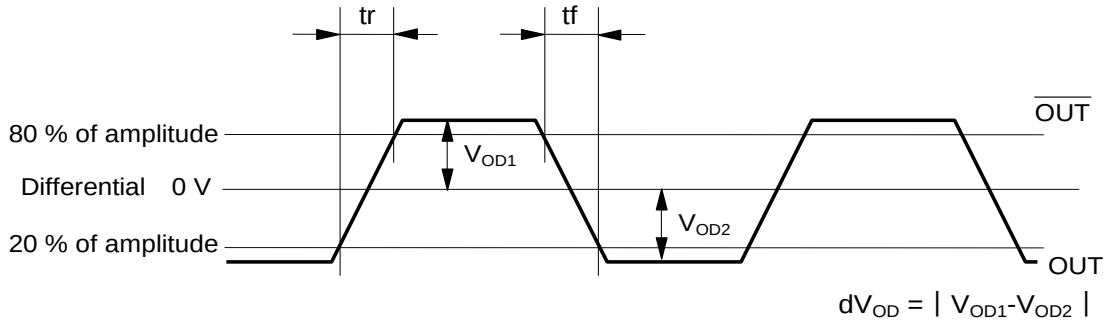
• Impedance of power supply should be as low as possible.

4.Timing chart

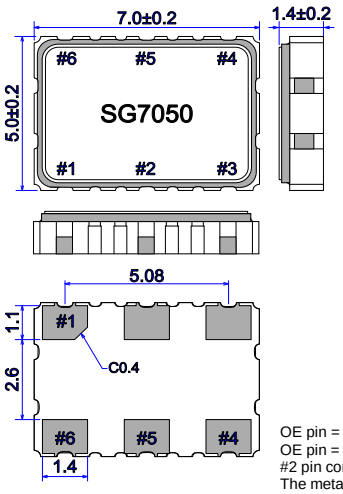
Each output waveform (OUT, and $\overline{OUT}$)



Differential output waveform (OUT – $\overline{OUT}$)



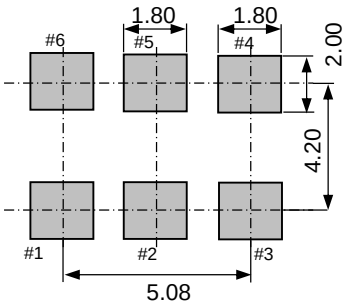
5.External dimensions (Unit: mm)



Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	VCC

OE pin = "H" or "open" : Specified frequency output.
OE pin = "L" : Output is high impedance.
#2 pin connection = GND is acceptable.
The metal cap is connected to #3 pin.

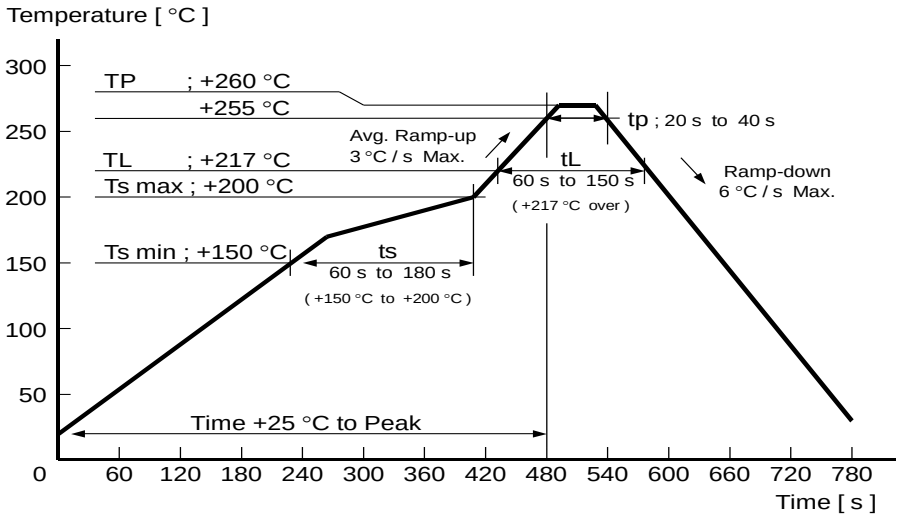
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

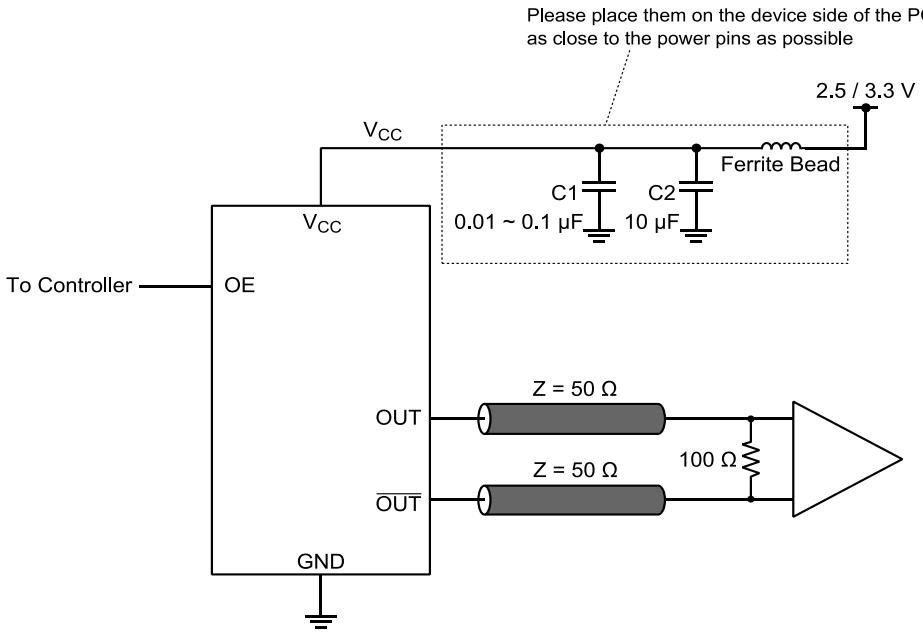
7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



8.Example of schematic layout

This figure shows an example of this product's application schematic.
As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.
In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible.
The component value of this filter is just an example, it may have to be adjusted.



* By-pass capacitor (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.
* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
* Please design the two output lines by characteristic impedance 100 Ω and same length, and try to make the output lines as short as possible.

9.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1G0042810016xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification

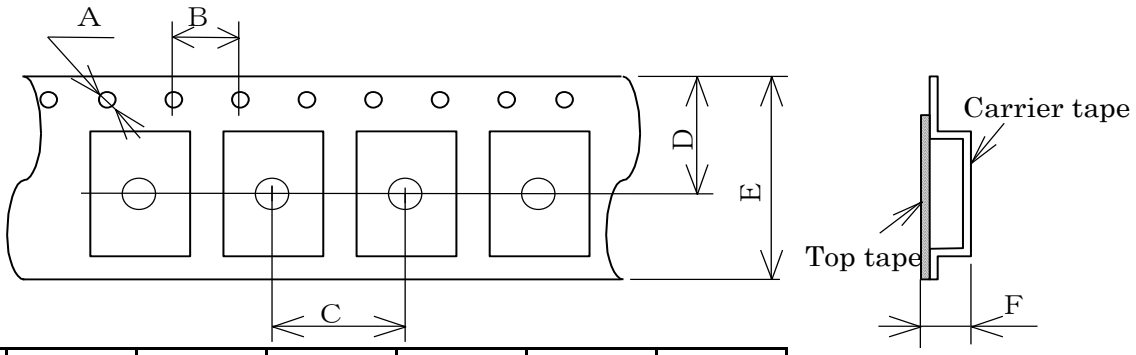
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

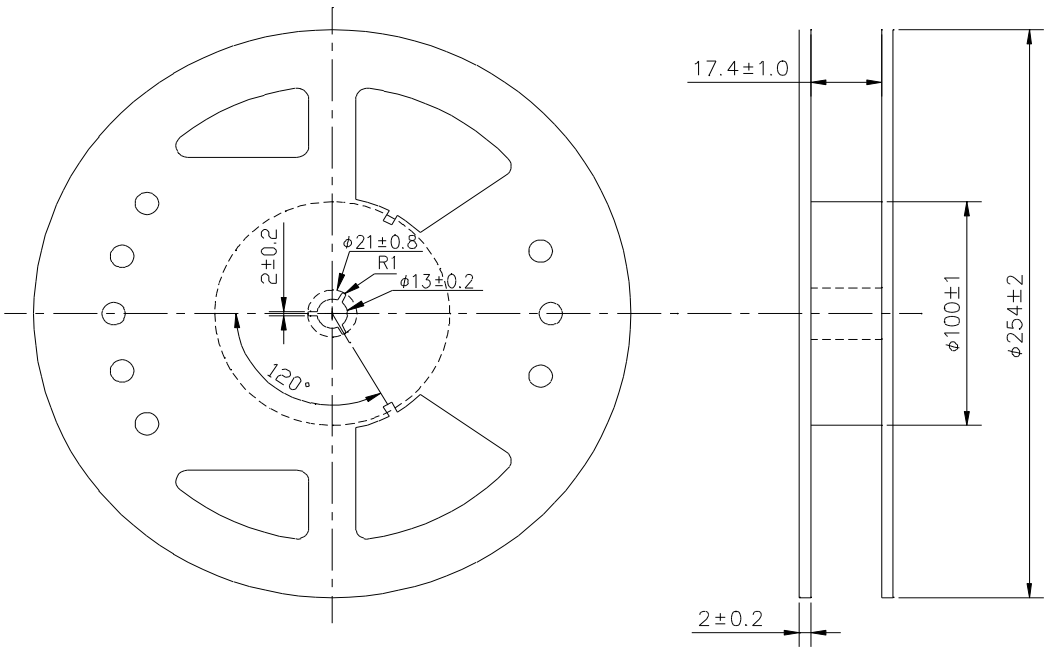


Symbol	A	B	C	D	E	F
Value	φ1.5	4	8	9.25	16	2.3

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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