# Clock OSC SG7050VAN

Product name SG7050VAN 125.003750MHz KJBA
Product Number / Ordering code X1G0042810119xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LVDS

Pb free / Complies with EU RoHS directive

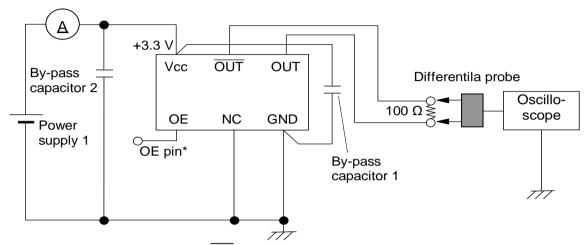
Reference weight Typ. 149 mg

1.Absolute maximum ratings									
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks			
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-			
Storage temperature	T_stg	-40	-	+125	°C	Storage as single product			
Input voltage	Vin	-0.3	-	Vcc+0.3	V	OE Terminal			

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks
Output frequency	f0	-	125.0038	-	MHz	
Supply voltage	Vcc	2.25	-	3.63	V	-
Operating temperature	T_use	-20	_	+70	°C	-
Frequency tolerance	f tol	-50	_	50	x10 <sup>-6</sup>	-
Current consumption	Icc	-	_	30	mA	OE = Vcc, L_LVDS = 100 Ω
Stand-by current	I std	-	_	_	mA	-
Disable current	I_dis	-	_	20.0	mA	OE = GND
Symmetry	SYM	45	_	55	%	At output crossing point
Output voltage(LVDS)	Vod	250	_	450	mV	-
	dVop	-	-	50	mV	1-
	Vos	1.15	-	1.35	V	1-
	dVos	-	-	150	mV	].
Output load condition(LVDS)	L_LVDS	-	100	-	Ω	Connected between OUT and OUT
Input voltage	V <sub>IH</sub>	70 % Vcc	-	-		-
	V <sub>IL</sub>	-	-	30 % Vcc		].
Rise time	t <sub>r</sub>	-	-	300	ps	-
Fall time	tf	-	-	300	ps	-
Start-up time	t_str	-	-	3	ms	-
Jitter	t <sub>DJ</sub>	-	8.3	-	ps	Deterministic Jitter Vcc=2.5V
	$T_{RJ}$	-	0.8	-	ps	Random Jitter Vcc=2.5V
	t <sub>RMS</sub>	-	5.3	-	ps	δ(RMS of total distribution) Vcc=2.5V
	t <sub>p-p</sub>	-	22	-	ps	Peak to Peak Vcc=2.5V
	t <sub>acc</sub>	-	1.1	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles Vcc=2.5V
Phase jitter	t <sub>PJ</sub>	-	0.34	-	ps	Offset Frequency: 12kHz to 20MHz Vcc=2.5V
Phase noise	L(f)	-	-53	-	dBc/Hz	Offset 1Hz Vcc=2.5V
		-	-85	-	dBc/Hz	Offset 10Hz Vcc=2.5V
		-	-111	-	dBc/Hz	Offset 100Hz Vcc=2.5V
		-	-123	-	dBc/Hz	Offset 1kHz Vcc=2.5V
		-	-132	-	dBc/Hz	Offset 10kHz Vcc=2.5V
		-	-138	-	dBc/Hz	Offset 100kHz Vcc=2.5V
		-	-138	-	dBc/Hz	Offset 1MHz Vcc=2.5V
Frequency aging	f_age	-5	-	5	x10 <sup>-6</sup> /Year	25 °C, 1st year
		-	-	-		-

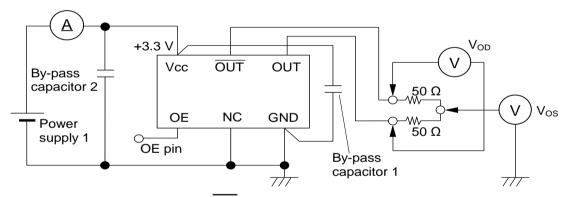
#### 3.Test circuit

1) To observe waveform and current (case 1)



- \* The lines from OUT and OUT pin are same length.
- \* To measure the disable current, OE pin is connected to GND

#### 2) To observe waveform and current (case 2)

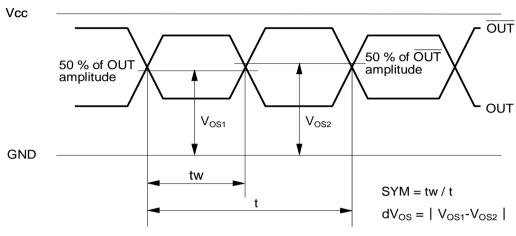


- \* The lines from OUT and OUT pin are same length.
- 3) Measurement condition
- A) Oscilloscope
- •Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- •Probe ground should be placed closely from test point and lead length should be as short as possible.
- B) By-pass capacitor 1 (approx. 0.01  $\mu F$  to 0.1  $\mu F$ ) places closely between Vcc and GND.
- C) By-pass capacitor 2 (approx. 10  $\mu F$ ) places closely between power supply terminals on the board.
- D) Use the current meter whose internal impedance value is small.
- E) Power supply
- Start up time (0 Vg90 %Vcc) of power source should be more than 150  $\mu$ s and slew rate should be less than 19.8 mV/ $\mu$ s.
- Impedance of power supply should be as low as possible.

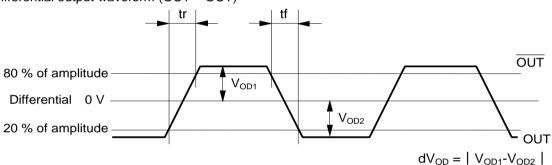
# 4.Timing chart

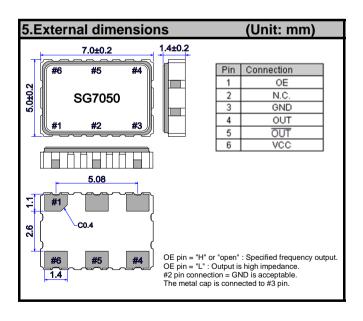
## **SEIKO EPSON CORPORATION**

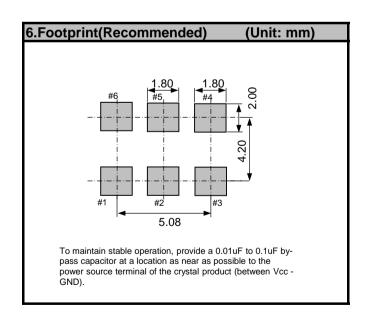
Each output waveform (OUT, and OUT)

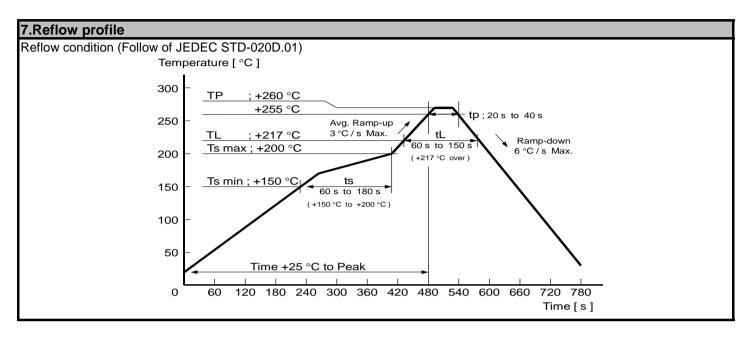


Differential output waveform (OUT - OUT)







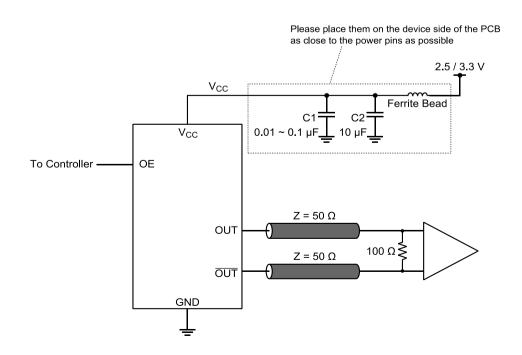


#### 8. Example of schematic layout

This figure shows an example of this product's application schematic.

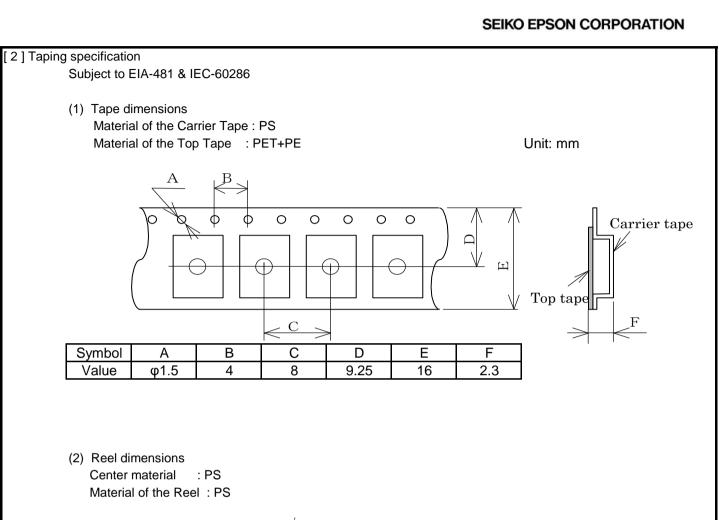
As with any high speed analog circuitry, the power supply pins for this device are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.



- $^*$  By-pass capacitor (approx. 0.01  $\mu F$  to 0.1  $\mu F$ ) places closely between Vcc and GND.
- \* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
- \* Please design the two output lines by characteristic impedance  $100 \Omega$  and same length, and try to make the output lines as short as possible.

#### 9.Packing information [ 1 ]Product number last 2 digits code(xx) description The recommended code is "00" X1G0042810119xx Code Condition Code Condition Any Q'ty vinyl bag(Tape cut) 500pcs / Reel 01 13 11 Any Q'ty / Reel 00 1000pcs / Reel 12 250pcs / Reel



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