Programmable VCXO/VCSO VG7050EAN

Product name VG7050EAN SM18T009 CJGHPZ
Product code / Ordering code X1G0045411009xx
Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform LV-PECL
Pb free / Complies with EU RoHS directive
Reference weight Typ.167mg

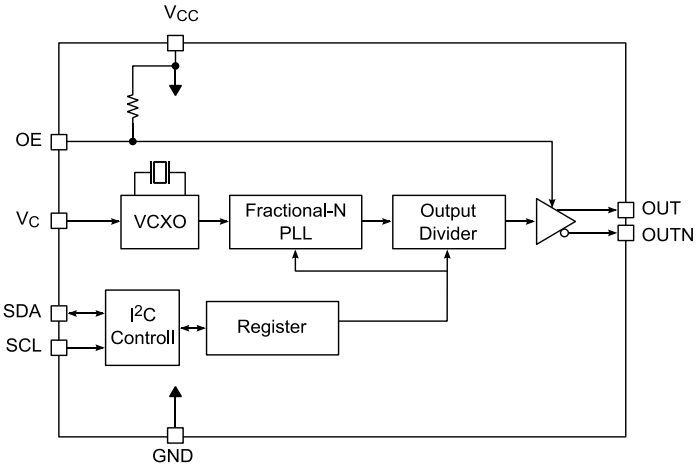
1.Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+4	V	-
Storage temperature	T_stg	-55	-	+125	ºC	-
Input voltage	Vin	GND-0.3	-	Vcc+0.3	V	Except SDA and SCL pin

2.Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		156.2500		MHz	Start-up frequency
Supply voltage	Vcc	2.97	3.3	3.63	V	-
Control voltage	Vc	0.3	1.65	3	V	Vc=1.65V+/-1.35V
Operating temperature	T_use	-40	-	+85	ºC	-
Frequency tolerance	f_tol	-50	-	+50	$x10^{-6}$	includes 10 years aging
Current consumption	Icc	-	-	90	mA	OE = Active L_ECL =50Ω
Disable current	I_dis	-	-	40	mA	OE inactive ,output standby:Hi-Z mode
Frequency control range	f_cont	-50 to +/-23	-	-	$x10^{-6}$	-
Absolute pull range	APR	+/-0 to +/-180			$x10^{-6}$	Programmable
Modulation characteristics	BW	10	-	-	kHz	+/-3 dB
Input resistance	Rin	5000	-	-	kΩ	DC Level
Frequency change polarity	-					Positive polarity
Symmetry	SYM	45	-	55	%	at outputs crossing point
Output voltage	V_{OH}	Vcc-1.025	-	-	V	-
	V_{OL}	-	-	Vcc-1.62	V	-
Output load condition	L_ECL	-	50	-	Ω	Outputs terminated to Vcc-2.0V
Input voltage	V_{IH}	70%Vcc	-	-	V	OE,SDA,SCL
	V_{IL}	-	-	30%Vcc	V	OE,SDA,SCL
Rise time	tr	-	-	0.4	ns	20 % to 80 % of amplitude
Fall time	tf	-	-	0.4	ns	20 % to 80 % of amplitude
Start-up time	t_str	-	-	10	ms	-
Phase noise	F_{CN}	-	-90	-	dBc/Hz	Offset 100Hz
		-	-115	-	dBc/Hz	Offset 1kHz
		-	-131	-	dBc/Hz	Offset 10kHz
		-	-132	-	dBc/Hz	Offset 100kHz
		-	-142	-	dBc/Hz	Offset 1MHz
Phase jitter	t_{PJ}	-	0.3	-	ps	@148.351648 MHz, Offset Frequency: 12kHz to 20MHz
Frequency aging	f_aging	-	-	-	$x10^{-6}$	Included in frequency tolerance

3.Block diagram

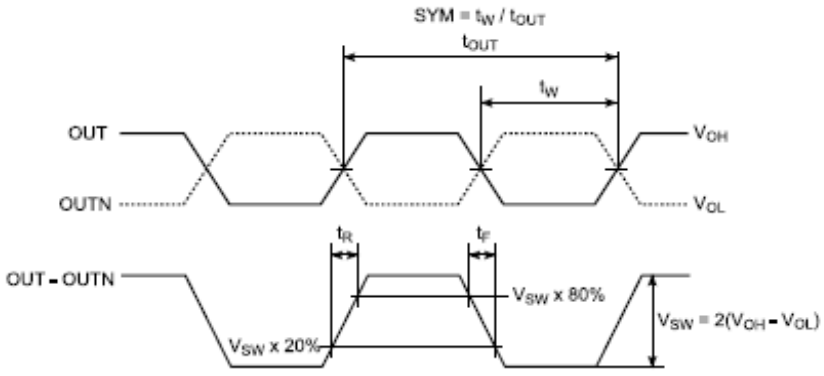


4.OE Function / OE Standby typ

OE Function	OE Standby Type	Frequency output OE pin	Oscillator Stop	
			OE pin	OUT,OUTN state
H: High Active	Z: High-Z	“H” or “OPEN”	“L”	High Impedance
L: Low Active		“L” or “OPEN”	“H”	
H: High Active	F: Fix	“H” or “OPEN”	“L”	OUT=”L”, OUTN=”H”
L: Low Active		“L” or “OPEN”	“H”	

3.Timing chart

Output wave form



Output Rise/Fall Time, Symmetry (duty cycle)

4.Test circuit

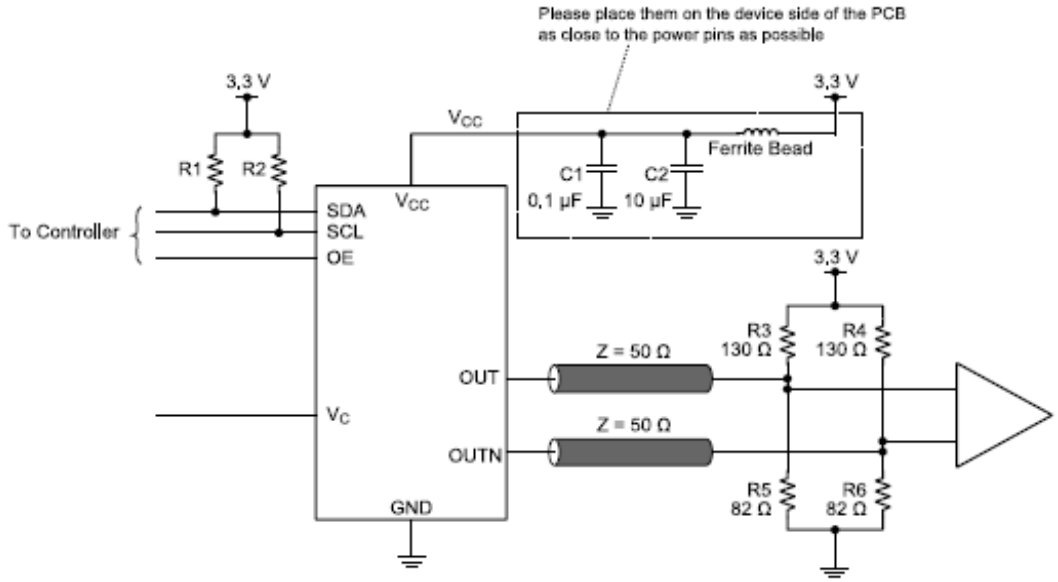
1) Condition

This figure shows an example of this product’s application schematic.

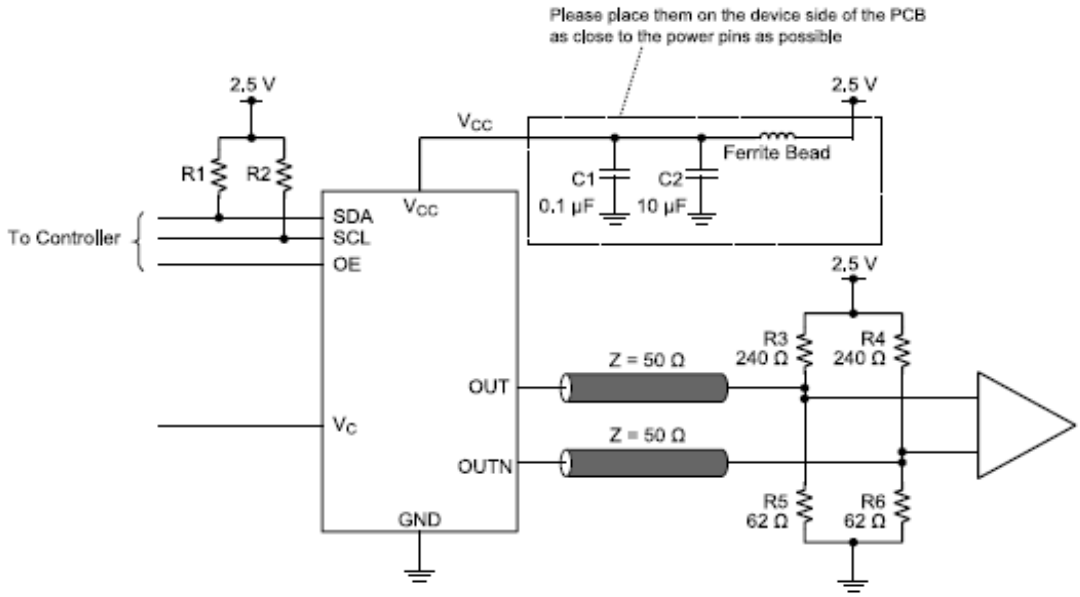
As with any high speed analog circuitry, the power supply pins for VG7050EAN are vulnerable to noise. In order to achieve optimum jitter performance, power isolation with filter device is required for power supply pins.

In order to achieve best performance of the power isolation filter, it is recommended that the filter composing devices is placed on the device side of the PCB as close to the power pins as possible. The component value of this filter is just an example, it may have to be adjusted.

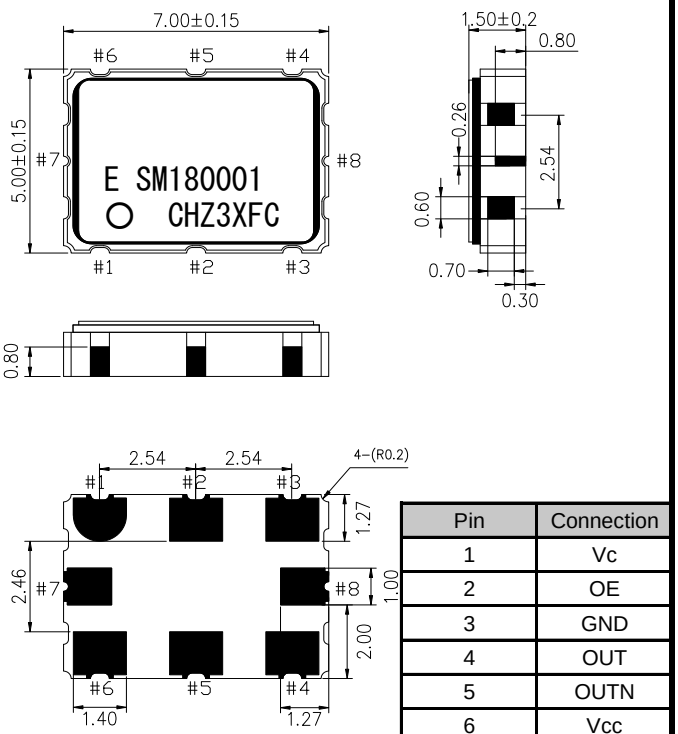
2)Vcc = 3.3V



3) Vcc = 2.5V

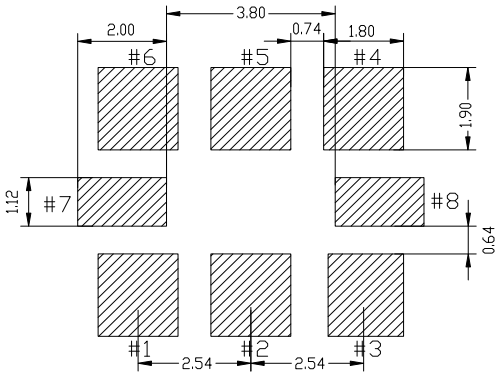


5.External dimensions (Unit: mm)



Pin	Connection
1	Vc
2	OE
3	GND
4	OUT
5	OUTN
6	Vcc
7	SDA
8	SCL

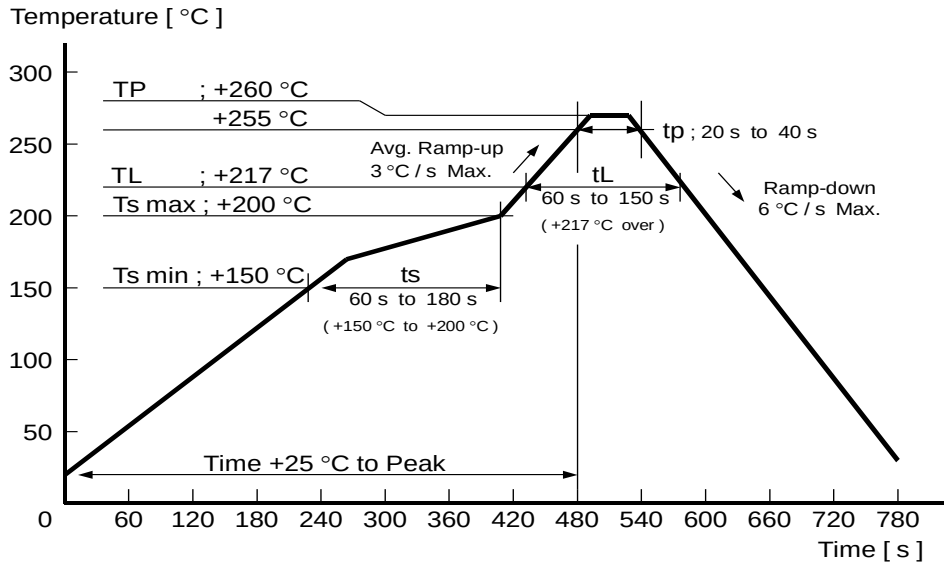
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



8.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1G0045411009xx

Code	Condition	Code	Condition
00	1000pcs / Reel	12	250pcs / Reel
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel		

[2] Taping specification

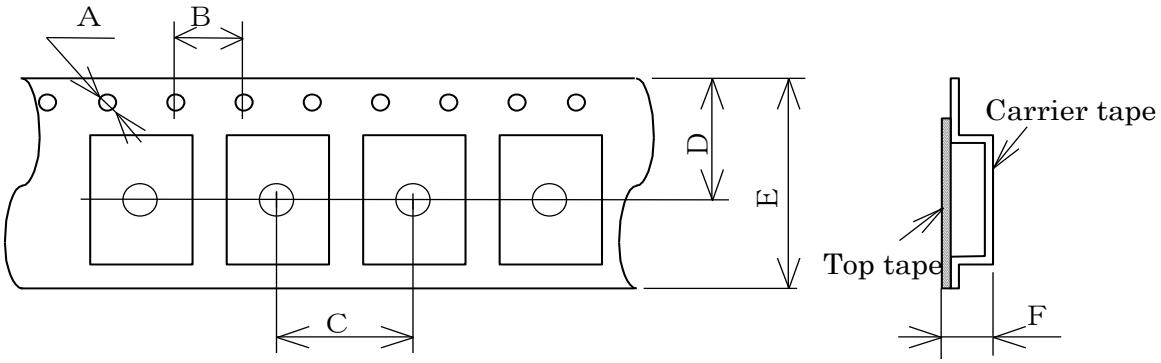
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

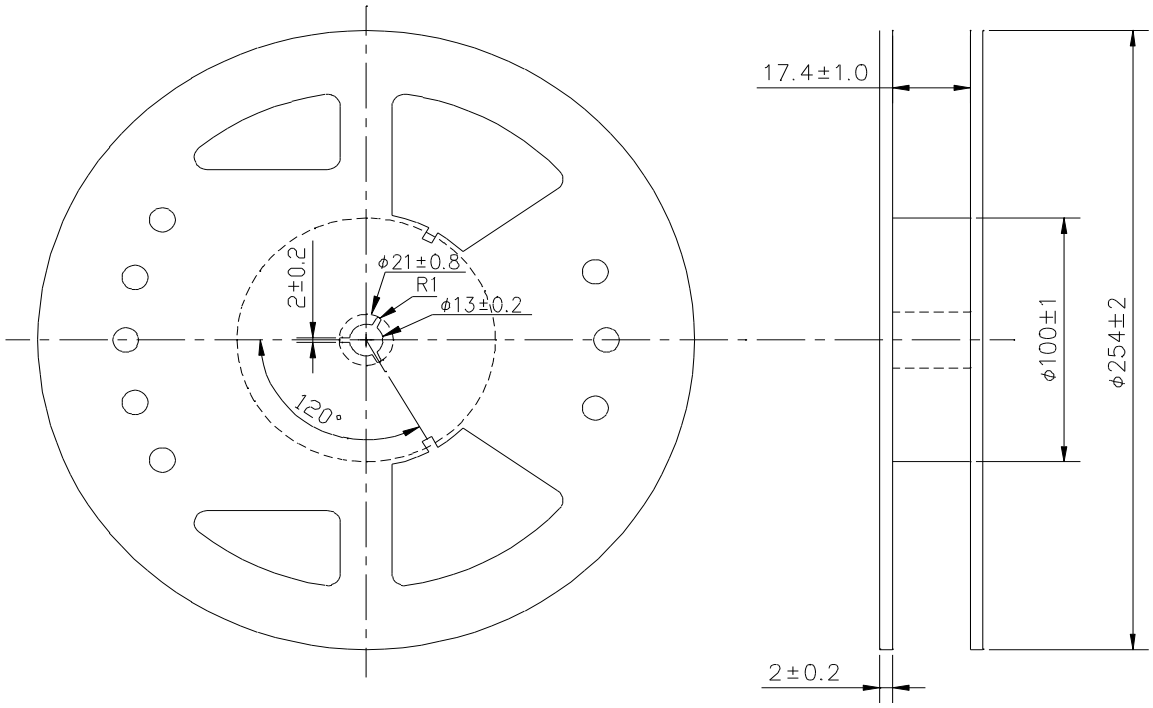


Symbol	A	B	C	D	E	F
Value	Φ1.5	4	8	9.25	16	2.3

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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